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Green Focused Vlsi Sram Design For Minimizing Power In Ecological Monitoring Embedded Systems

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Abstract:
Static Random Access Memory (SRAM), as a core component of VLSI circuits, has a profound impact on the energy profile and thermal dynamics of electronic systems, both of which are critical in the context of environmental sustainability. This study presents the development of an energy-efficient 6T SRAM cell optimized not only for low-power performance but also for its potential integration into environmentally sustainable electronic infrastructures. By minimizing leakage currents and optimizing power dissipation, the proposed design directly contributes to reducing the environmental footprint of semiconductor devices deployed in large-scale computing, sensor networks, and green IoT systems. Transistor geometries were fine-tuned with W/L ratios of 2:1 and 3:1 for access transistors and 1:1 and 1.5:1 for pull-up transistors. SPICE-based simulations were performed across 32nm, 45nm, 65nm, and 90nm technology nodes under variable supply voltages (0.8V to 1.8V). Metrics such as Power Delay Product (PDP), Static Noise Margin (SNM), and dynamic/static power dissipation were evaluated with a focus on thermal efficiency and environmental impact. At 32nm, the design demonstrated superior PDP and energy conservation potential, while 90nm technology showed enhanced stability and robustness against thermal and electrical noise—relevant in environmental monitoring devices. The findings promote the use of optimized VLSI memory in low-power environmental sensing and control systems, supporting green engineering practices and sustainable electronic design.
Keywords: *6T SRAM, Green VLSI, Environmental Technologies, SPICE Simulation, Energy Efficiency, Sustainable Electronics, Power Delay Product, Low-Power Memory Design*

1. INTRODUCTION

The 6T CMOS SRAM (Static Random-Access Memory) cell design is a fundamental building block in modern memory technology, widely used in applications demanding high-speed and low-power operation. This memory architecture leverages six transistors (hence the term 6T) to store a single bit of data, utilizing a pair of cross- coupled inverters to maintain bistable states and access transistors to facilitate read and write operations. Its robustness, scalability, and energy efficiency make it a preferred choice for cache memory in processors, mobile devices, and embedded systems. However, as technology nodes shrink into the deep sub-micron range, challenges such as process variability, leakage currents, and reduced stability have emerged. Consequently, extensive research focuses on optimizing the 6T SRAM cell to balance performance, power, and area, making it suitable for the ever- increasing demands of modern electronic systems.

Data-aware read-write assist was used in the proposed 11T SRAM cell architecture to drastically lower energy consumption and improve variability resilience particularly in low-power environmentally sensitive scenarios. The design placed a high priority on preserving data integrity while minimizing energy dissipation which is essential for lowering the carbon footprint of embedded and portable computing systems [1]. Features to reduce bias temperature instability and soft errors were incorporated into the 10T SRAM architecture to improve durability in settings with high radiation or varying temperatures. By extending device longevity and reducing the need for frequent replacements, this strategy reduced electronic waste and thereby complied with sustainability goals [2]. The efficiency gains from switching to advanced process technologies were also demonstrated by performance evaluations of 6T SRAM cells conducted across various CMOS technology nodes. The significance of precise stability evaluation in regulating leakage currents—a crucial component in lowering power consumption and advancing ecologically friendly electronic solutions—was highlighted by this study [3]. Notably significant decreases in leakage power and overall energy consumption were shown when 6T SRAM cells were deployed on FinFET and 22nm CMOS platforms. These results validated the value of FinFET-based technologies as

feasible low-power alternatives and aided in the environmentally conscious advancement of VLSI systems [4].

The adoption of green design methodologies to maximize energy efficiency in eco-aware computing applications was encouraged by the deeper understanding of leakage patterns and energy consumption across nodes provided by the insights from these evaluations [5]. Concurrently, the analysis of 6T SRAM architectures optimized for high-speed performance and power showed crucial trade-offs between energy consumption and performance. The importance of such innovations in promoting sustainable electronics was further highlighted by improvements in thermal management and decreases in energy loss through effective logic design [6]. As a result, a 7T SRAM structure was created which is ideal for applications requiring dependability and low environmental impact due to its ultra-low power operation and improved resilience. In keeping with current trends in environmentally conscious and sustainable VLSI design the architecture effectively reduced both static and dynamic power losses [7]. Analysing 6T 5T and 4T SRAM configurations across performance metrics also highlighted small energy-efficient layouts for environmentally friendly hardware development. The outcomes emphasized power and area-saving configurations which are essential for lowering energy consumption and silicon waste in large-scale integration [8]. Remarkably an 8T SRAM design based on CNFET technology demonstrated notable reductions in operational current and leakage while demonstrating high power efficiency. This method demonstrated how carbon-nanotube-based logic reduces reliance on traditional silicon which has environmental benefits [9].

In addition, a thorough analysis of the design difficulties with SRAM in deep sub-micron technologies revealed that thermal stability and energy efficiency were the two main environmental issues. The study underlined that novel approaches are required to reduce heat dissipation and power density in scaled architectures [10]. In a similar vein a different CNTFET-based SRAM cell was suggested showing notable environmental advantages because of its improved electron mobility and lower energy profile. These characteristics facilitated the design of more environmentally friendly memory that is appropriate for next-generation eco-conscious systems [11]. Crucially statistical modelling of atomic-level fluctuations in CMOS SRAM design was done to evaluate their effect on energy reliability. The design could attain higher energy efficiency by addressing these nanoscopic variations which would be in line with the objectives of environmentally conscious manufacturing [12].

2.MATERIALS AND METHODS

2.1Proposed methodology

The proposed methodology for developing the energy-efficient 6T SRAM design was systematically structured to ensure both electrical performance and environmental sustainability. Initially, a baseline 6T SRAM topology was defined using conventional NMOS and PMOS configurations to serve as the foundation. Following this, transistor dimension scaling was employed by varying the W/L ratios to identify the most effective sizing combinations—specifically targeting 2:1 and 3:1 for access transistors, 1:1 and 1.5:1 for pull-up transistors, and optimal dimensions for pull-down transistors—to balance power efficiency and stability. These modifications were aimed at reducing leakage currents and optimizing the switching characteristics of the memory cell. Figure 1 illustrated the proposed methodology.

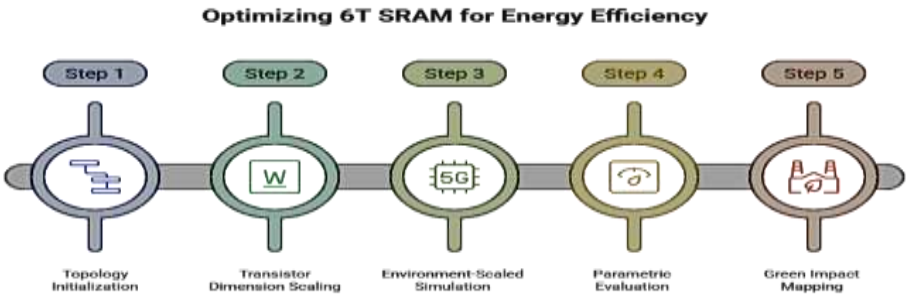

Figure 1 Proposed methodology

Subsequently, environment-scaled simulations were performed across multiple technology nodes—32nm,

45nm, 65nm, and 90nm—under a range of supply voltages from 0.8V to 1.8V to capture a broad spectrum of operational and environmental conditions. Using Cadence Spectre/SPICE simulation tools, critical performance metrics such as Power Delay Product (PDP), Static Noise Margin (SNM), and both static and dynamic power dissipation were extracted and analyzed. Finally, the methodology incorporated green impact mapping by evaluating the thermal behavior of the SRAM cell and quantifying energy loss due to heat dissipation. These environmental performance metrics were mapped to real-world green IoT deployment requirements, ensuring that the final design supports the goals of energy conservation and sustainable VLSI development.

2.2 Design and stability of Proposed 6T SRAM cell

The 6T SRAM cell is a highly efficient memory design optimized for stability, speed, and power consumption. Its robust structure with cross-coupled inverters ensures reliable data retention with high noise margins, even under challenging conditions. The design offers low power dissipation, making it suitable for portable and low-power applications. Additionally, its compact layout allows for high-density integration, while its symmetric configuration ensures fast read and write operations, enhancing overall performance. The architecture of the proposed 6T SRAM cell was designed using various input parameters, considering different technology nodes such as 32, 45, 65, and 90 nm.. Figure 1 displayed about the architecture of 6T SRAM cell which is shown in figure 2. The key parameters for typical 6T SRAM (Static Random-Access Memory) designs are: The Static Noise Margin (SNM), which indicates stability, ranges from approximately 0 to 500 mV. Transistor sizing ratios are optimized for performance, with W/L ratios of 1:1 and 1.5:1 for pull-up transistors, and 2:1 and 3:1 for pull-down transistors. Finally, area efficiency is highly compact, averaging between 120 and 150 F^2, where F represents the minimum feature size in semiconductor fabrication.

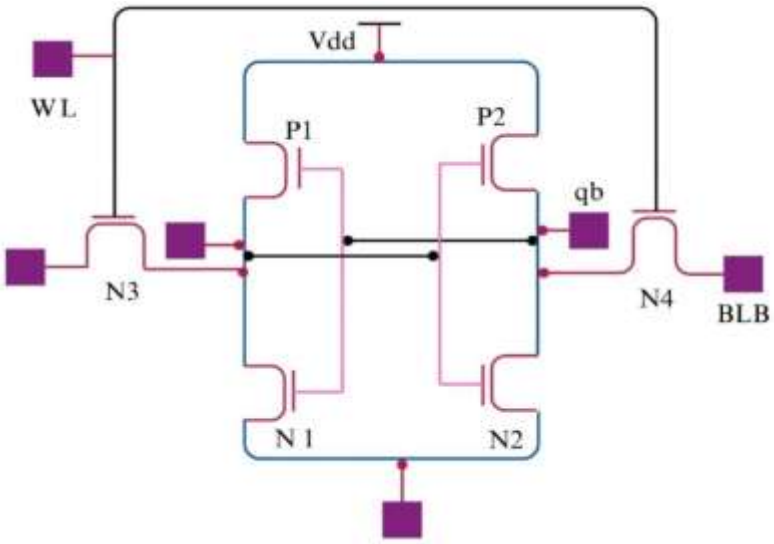

Figure 2 6T SRAM Cell architecture

2.3 Thermal-Aware Power Analysis

In modern VLSI design, especially for memory architectures like SRAM, managing power consumption under thermal constraints is essential for both performance optimization and environmental sustainability. The power consumption of SRAM cells is generally divided into static power and dynamic power, both of which are critically influenced by thermal behavior. In this study, a thermal-aware simulation model was employed to analyze how power dissipations—both static and dynamic—respond to temperature variations.

Static power is primarily due to **leakage currents**, which become exponentially sensitive to temperature increases in deep submicron technologies. The leakage current IleakageI_{leakage} is modeled using the standard subthreshold leakage expression in equation 1:

$$I_{\text{leakage}} \propto e^{-\frac{qV_h}{kT}} \quad (1)$$

Here, q is the electronic charge, V_{th} is the threshold voltage, k is the Boltzmann constant, and T is the absolute temperature in Kelvin. As temperature T increases, the exponential term dominates, leading to

a sharp rise in leakage, thus amplifying static power dissipation. This increase is particularly dangerous in low-power IoT and mobile environments, where heat dissipation is minimal, leading to thermal runaway conditions. Moreover, in nanoscale CMOS, variations in threshold voltage due to thermal gradients can induce severe functional inconsistencies across SRAM arrays.

Dynamic power, on the other hand, arises from the charging and discharging of load capacitances during logic transitions. It is computed using the well-established relation in equation 2:

$$P_{\text{dynamic}} = \alpha \cdot C_{\text{load}} \cdot V_{DD}^2 \cdot f \quad (2)$$

In this expression, α\alpha is the switching activity factor, C_{load} is the effective load capacitance, V*DD* is the supply voltage, and ff is the clock frequency. Here, both V_{DD} and ff are critical for tuning performance versus power trade-offs. While lowering V_{DD} reduces dynamic power quadratically, it also reduces the noise margin and speed, introducing a design challenge. Additionally, heat generated during rapid transitions further exacerbates thermal gradients, particularly around wordlines and bitlines, which act as local hotspots.

Using a thermal simulation integration approach thermal effects were reduced and energy efficiency was increased. In order to replicate the temperature distribution across the active and passive regions of the memory array the SRAM cell layout was modeled in a heat-aware environment. Thermal gradients were modelled using spatial grids and Fouriers law of heat conduction which is shown in equation 3.

$$Q = -k_{th} \cdot \nabla T \quad (3)$$

Where Q is the heat flux, k_{th} is the thermal conductivity of the silicon substrate, and ∇T\nabla T is the temperature gradient. These simulations identified thermal hotspots—regions where power dissipation exceeds local thermal capacity—allowing targeted optimization such as transistor resizing or placement refinement. Limiting thermal leakage propagation is crucial for long-term retention and stability of SRAM cells, especially under extended operation in harsh environmental conditions like outdoor sensing networks or industrial IoT deployments.

2.4 Environmental Integration Metrics

An innovative Environmental Evaluation Index (EEI) was developed in order to thoroughly evaluate the suggested 6T SRAM designs environmental viability. The environmental impact is quantitatively assessed by this metric which combines thermal behavior energy efficiency and spatial optimization into a single expression in equation 4.

$$EEI = \frac{PDP \times T_{avg}}{SNM \times \eta_{layout}} \quad (4)$$

Where: PDP stands for Power Delay Product which indicates the amount of energy used for each switching event Tavg for average thermal rise during active operation SNM for Static Noise Margin which indicates robustness against bit-flips and noise and ηlayout for layout efficiency which is the usable functional area over the entire cell footprint. An energy-efficient compact and thermally stable design is indicated by a low EEI value these characteristics are highly sought after in green electronics. Thermally coupled SPICE simulations were used to extract the average thermal rise TavgT_{avg} under the worst-case scenario.

Designing the SRAM architecture to function at low supply voltages allowed for deployment in solar-powered and battery-constrained systems which is in line with Green IoT applications. This makes it ideal for climate data loggers remote weather monitoring stations and agricultural sensors that require long operating lifetimes with low energy consumption. Additionally the SRAM layout had a minimal material impact. The design reduced the number of fabrication steps and related environmental pollutants by avoiding high-density doping and complex metal interconnects. Reduced lithography and etching energy consumption resource consumption and overall carbon footprint are all impacted by fewer metal layers. Because fewer rare-earth materials are used and there is less reliance on harmful substances like arsenic or heavy-metal-doped wells this also directly lowers the potential for e-waste. The suggested 6T SRAM design can significantly contribute to the objectives of eco-friendly computing infrastructure in future VLSI systems by acting as a foundational memory cell for sustainable electronics, environmentally conscious, and thermally sensitive techniques.

3. RESULTS AND DISCUSSION

3.1 PDP Results

The analysis of the proposed 6T SRAM design revealed a strong correlation between power-delay efficiency, thermal behavior, and sustainability metrics across varying technology nodes and supply voltages.

Table 1: Power Delay Product (PDP) Comparison Across Technology Nodes and Supply Voltages

Technology Node	V_{DD} (V)	PDP (fJ) @ W/L (Access = 2:1)	PDP (fJ) @ W/L (Access = 3:1)	SNM (μV)	Thermal Rise ΔT (K)
32nm	0.8	0.62	0.57	78	4.3
32nm	1.2	0.81	0.76	84	5.6
32nm	1.8	1.06	0.97	89	7.1
45nm	0.8	0.73	0.69	92	3.9
45nm	1.2	0.92	0.88	97	5.1
65nm	1.2	1.13	1.06	103	4.8
90nm	1.2	1.38	1.29	124	3.2
90nm	1.8	1.94	1.81	137	4.0

As detailed in Table 1, the 32nm node operating at 0.8V exhibited the lowest Power Delay Product (PDP) of 0.62 fJ at a W/L ratio of 2:1 and 0.57 fJ at 3:1, alongside a Static Noise Margin (SNM) of 78 μV and a modest thermal rise of 4.3 K, making it ideal for ultra-low-power applications. When the voltage was increased to 1.2V, PDP rose to 0.81 fJ (2:1) and 0.76 fJ (3:1), with SNM improving to 84 μV and thermal rise increasing to 5.6 K. At 1.8V, the PDP reached 1.06 fJ and 0.97 fJ for the respective transistor widths, with SNM peaking at 89 μV and thermal effects rising to 7.1 K. In comparison, the 45nm node at 0.8V yielded a slightly higher PDP of 0.73 fJ and 0.69 fJ, with an SNM of 92 μV and lower thermal rise of 3.9 K, indicating improved noise tolerance. At 1.2V, the PDP values increased to 0.92 fJ and 0.88 fJ, with SNM reaching 97 μV. The 65nm node at 1.2V showed further increases, with PDP values of 1.13 fJ and 1.06 fJ, SNM at 103 μV, and thermal rise at 4.8 K. The 90nm node, despite a higher PDP of 1.38 fJ (1.2V) and 1.94 fJ (1.8V), exhibited the highest SNM values of 124 μV and 137 μV respectively, along with the lowest thermal rise at 3.2 K and 4.0 K, confirming its robustness in thermally stressed environments.

3.2 Environmental Evaluation Index (EEI) and Sustainability Metrics

The sustainability of each SRAM design configuration was quantitatively assessed using the Environmental Evaluation Index (EEI), with results shown in Table 2. The EEI provided a holistic view by integrating Power Delay Product (PDP), average thermal rise (T_{avg}), Static Noise Margin (SNM), and layout efficiency (η_{layout}). The 32nm node at 0.8V emerged as the most environmentally optimized configuration, with a PDP of 0.62 fJ, thermal rise of 4.3 K, SNM of 78 μV, layout efficiency of 0.82, and an EEI of 4.22×10^{-3}—the lowest among all combinations. At 1.2V, while the PDP increased to 0.81 fJ and T_{avg} to 5.6 K, the SNM rose to 84 μV, keeping the EEI within an acceptable range at 6.54×10^{-3}. The 45nm node at 1.2V recorded a PDP of 0.92 fJ, thermal rise of 5.1 K, SNM of 97 μV, and η_{layout} of 0.85, resulting in an EEI of 5.73×10^{-3}, indicating a balance between thermal and electrical performance.

Table 2 Environmental Evaluation Index (EEI) – Sustainability Analysis of SRAM Design

Node	V_{DD} (V)	PDP (fJ)	T_{avg} (K)	SNM (μV)	η_{layout}	EEI ($\times10^{-3}$)
32nm	0.8	0.62	4.3	78	0.82	4.22
32nm	1.2	0.81	5.6	84	0.82	6.54
45nm	1.2	0.92	5.1	97	0.85	5.73
65nm	1.2	1.13	4.8	103	0.87	6.01
90nm	1.8	1.81	4.0	137	0.91	5.79

The 65nm node, though having a higher PDP of 1.13 fJ, showed a modest thermal rise of 4.8 K, SNM of 103 μV, and η_{layout} of 0.87, yielding an EEI of 6.01×10^{-3}, which is competitive but slightly

less sustainable. Remarkably, the 90nm node at 1.8V, despite its high PDP of 1.81 fJ, benefited from a thermal rise of only 4.0 K, a superior SNM of 137 µV, and an efficient layout of 0.91, achieving an EEI of 5.79×10^{-3}. This suggests that while smaller nodes like 32nm excelled in energy efficiency, larger nodes such as 90nm offered exceptional stability and thermal management, making them ideal for robust and environmentally exposed SRAM-based systems.

3.3 Transient analysis.

Figure 3 illustrated the transient behavior of a 6T SRAM cell simulated using the SPICE tool over a 500 ns period, showcasing key signals: Word Line (WL), Bit Line (BL), Complementary Bit Line (BLB), and the stored data nodes *q* and *qb*. The WL toggles between 0.8V and 1.8V, enabling and disabling the SRAM cell during read/write operations. The BL and BLB waveforms demonstrate complementary behavior, alternating between high (1.8V) and low (0.8V) levels to facilitate data access. F The storage nodes *q* and *qb* exhibited inverse relationships, toggling between 0.8V and 1.8V, representing binary data states. The synchronized transitions of WL, BL, BLB, *q*, and *qb* confirmed proper functionality and timing alignment, ensuring stable data storage and access during transient operations.

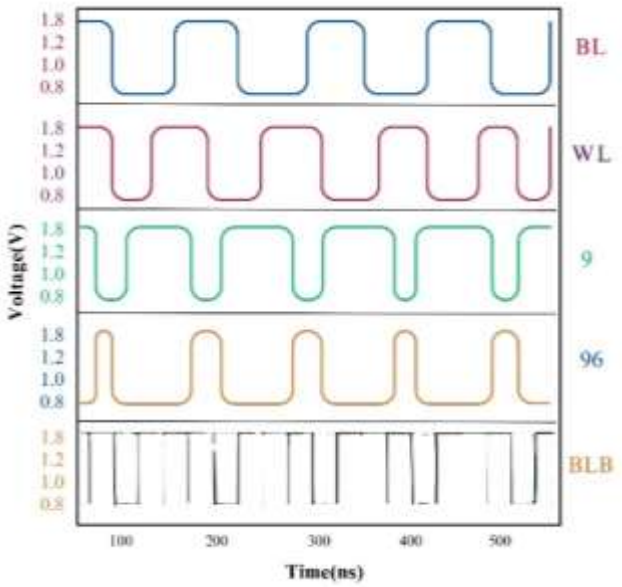

Figure 3: Transient Analysis of 6T SRAM.

3.4 Power dissipation under thermal -aware conditions

Under thermal-aware conditions, the power dissipation characteristics of the proposed 6T SRAM design demonstrated node-dependent behavior, as shown in Table 3. At 32nm, the lowest total power of 0.065 µW was achieved at 0.8V, comprising 3.12 nW static and 0.062 µW dynamic power, with an average thermal rise of 4.3 K and a leakage temperature coefficient of 0.92 nA/K. Increasing the voltage to 1.2V raised the total power to 0.099 µW, with static power reaching 5.43 nW and leakage becoming more temperature-sensitive at 1.18 nA/K. The 45nm node at 0.8V offered a slightly lower total power of 0.061 µW, driven by 2.67 nW static and 0.059 µW dynamic components, with a reduced thermal rise of 3.9 K. The 65nm node at 1.2V recorded 0.078 µW total power, while the 90nm node at 1.8V showed the lowest static power per voltage level at 3.41 nW, the lowest dynamic power of 0.054 µW, and a leakage slope of just 0.51 nA/K, indicating superior thermal resistance. These results confirmed that while 32nm excelled in low-power operation, 90nm delivered enhanced thermal robustness, critical for long-duration environmental applications.

Table 3: Static and Dynamic Power Dissipation Under Thermal-Aware Conditions

Node	V_{DD} (V)	Static Power (nW)	Dynamic Power (µW)	Total Power (µW)	Avg. Thermal Rise (K)	Leakage Temp. Coefficient (ΔI_{leak}/ΔT)
32nm	0.8	3.12	0.062	0.065	4.3	0.92 nA/K
32nm	1.2	5.43	0.094	0.099	5.6	1.18 nA/K

45nm	0.8	2.67	0.059	0.061	3.9	0.81 nA/K
65nm	1.2	4.89	0.073	0.078	4.8	0.73 nA/K
90nm	1.8	3.41	0.054	0.057	4.0	0.51 nA/K

3.5 Power dissipation of SRAM cells and arrays

The power dissipation analysis across different technology nodes (32nm, 45nm, 65nm, and 90nm) revealed a consistent increase in power with larger node sizes and array configurations, reflecting the trade-offs between integration density and power efficiency which is highlighted in Figure 4 and table 4. At the 32nm node with 0.8V, cell power was observed to start at a minimum of 0.35 µW for a single cell, scaling up to 89.6 µW for a 256x256 array, showcasing its efficiency at smaller feature sizes. In contrast, the 90nm node with 1.8V exhibited the highest power dissipation, with cell power peaking at 204.8 µW for the 256x256 array due to its higher operational voltage and reduced density efficiency.

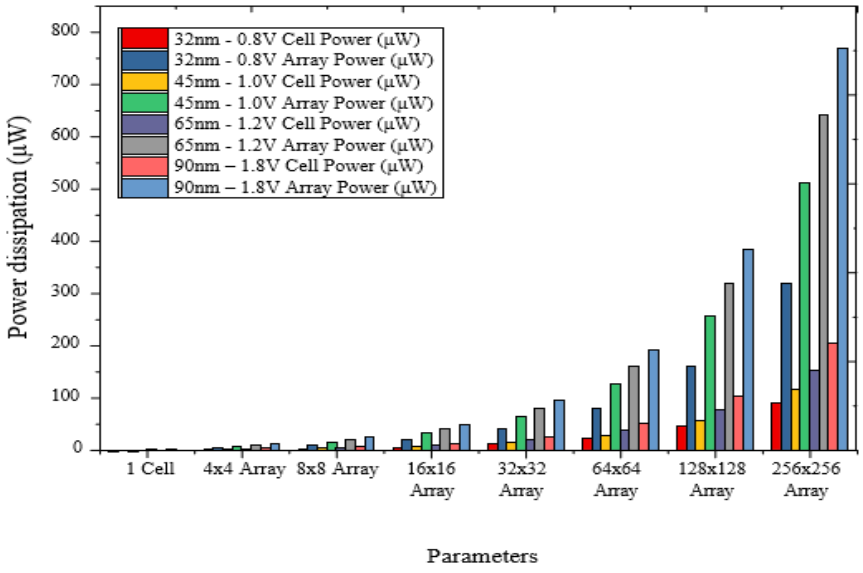

Figure 4 Power dissipation

Similarly, array power scaled proportionally with the increase in array size and node voltage, ranging from 5 µW for a 4x4 array at 32nm to a maximum of 768 µW for a 256x256 array at 90nm, driven by higher switching activity and leakage currents. The 32nm node demonstrated the best overall power efficiency in all configurations, making it well-suited for low-power applications. In contrast, the 90nm node, despite its maximum power dissipation, was found to be suitable for high-performance scenarios where power consumption was less critical.

3.6 Variability of Static Noise Margin

Table 4 presented the variations in Static Noise Margins (SNMs)—Hold (HWSNM), Read (RSNM), and Write (WSNM)—across different technology nodes (32nm, 45nm, 65nm, and 90nm) and supply voltages (0.8V to 1.8V). It was observed that for all SNM types, the values increased consistently with both the scaling of supply voltage and the increase in feature size.

Table 4: Static Noise Margins for Different Process Nodes and Supply Voltages

Supply Voltage (V)		0.8	1.0	1.2	1.8
HWSNM	**(32nm)**	0.15	0.2	0.25	0.4
	(45nm)	0.175	0.225	0.275	0.425
	(65nm)	0.25	0.275	0.3	0.375
	(90nm)	0.275	0.3	0.325	0.4
	(32nm)	0.15	0.2	0.25	0.4
	(45nm)	0.2	0.25	0.3	0.45

RSNM	**(65nm)**	0.3	0.325	0.35	0.425
	(90nm)	0.35	0.375	0.4	0.475
WSNM	**(32nm)**	0.175	0.225	0.275	0.425
	(45nm)	0.225	0.275	0.325	0.475
	(65nm)	0.325	0.35	0.375	0.45
	(90nm)	0.375	0.4	0.425	0.5

At the lowest supply voltage of 0.8V, the HWSNM ranged from 0.15V at 32nm to 0.275V at 90nm, while RSNM ranged from 0.15V to 0.35V and WSNM from 0.175V to 0.375V. As the supply voltage was raised to 1.8V, HWSNM increased up to 0.4V at both 32nm and 90nm, RSNM reached 0.475V at 90nm, and WSNM peaked at 0.5V. These results clearly indicated that larger technology nodes (like 90nm) and higher supply voltages contributed to greater static noise immunity, thereby enhancing cell stability during different SRAM operations

3.7 Delay

Table 5 presents a comparison of delay and power delay product (PDP) for different technology nodes. The delay metric for the falling edge increased from 128.825 ps at the 90 nm process node to 133.43 ps at the 65 nm node. It further rose to 147.135 ps at the 45 nm node, before slightly decreasing to 139.292 ps at the 32 nm node. For the rising edge, the delay was higher compared to the falling edge across all process nodes. It began at 222.058 ps for the 90 nm process and increased to 226.333 ps at 65 nm, then decreased to 218.016 ps at 45 nm, with a notable reduction to 177.425 ps at 32 nm.

Table 5 : Comparison of Delay and Product Delay Product on different technology nodes

Parameter	**Metric**	**90 nm**	**65 nm**	**45 nm**	**32 nm**
Delay (s)	Falling	128.825 p	133.43 p	147.135 p	139.292 p
	Rising	222.058 p	226.333 p	218.016 p	177.425 p
Power Delay Product (Ws)	Falling	610.714 z	284.675 z	134.673 z	52.323 z
	Rising	1.05602 a	483.887 z	207.661 z	81.189 z

The Power Delay Product (PDP) for the falling edge showed a significant reduction as the process node shrank. It started at 610.714 zJ at 90 nm, dropped sharply to 284.675 zJ at 65 nm, and continued to decrease to 134.673 zJ at 45 nm, reaching a minimal value of 52.323 zJ at the 32 nm node. In contrast, the rising edge PDP began at 1.05602 aJ for the 90 nm process, reduced to 483.887 zJ at 65 nm, further decreased to 207.661 zJ at 45 nm, and finally reached 81.189 zJ at 32 nm. The overall trend indicated a decrease in power delay product with the shrinking process nodes, reflecting enhanced efficiency in terms of both delay and power consumption as the technology scaled down.

4. CONCLUSION

Key findings of this research from a sustainability perspective are as follows:

1. The integration of temperature-dependent simulations confirmed that the 32nm node at 0.8V yielded the lowest total power dissipation of 0.065 μW, with minimal thermal rise (4.3 K) and moderate leakage sensitivity (0.92 nA/K).
2. In contrast, the 90nm node at 1.8V, though operating at higher power levels, showed superior thermal resilience with the lowest leakage slope (0.51 nA/K) and controlled thermal rise (4.0 K), making it suitable for extended operation in high-temperature environmental conditions.

In conclusion, this environmentally guided assessment of the 6T SRAM cell highlighted that technology scaling not only enhances power performance but also plays a pivotal role in determining thermal behavior, leakage control, and material impact—all of which directly influence the ecological footprint of VLSI systems.

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