

Design And Analysis of Low-Noise Amplifiers for High-Speed Analog VLSI Applications

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Abstract

Low-noise amplifiers (LNAs) constitute an vital part in contemporary high-speed analog VLSI circuits where noise suppression and gain tuning have direct implications on performance in wireless communications and high-frequency data processing. This work introduces the plan, simulation, and analysis of a CMOS-based amplifier designed to be optimized for high-speed analog VLSI applications. The target design combines current-reuse circuit techniques as well as the source-degeneration approaches to realize low noise figures and high linearity. The simulation results show a gain of 18.6 dB, noise figure of 2.1 dB, and power consumption of 4.5 mW at supply voltage of 1.2 V, making the design appropriate for future-generation high-speed analog systems. The results are confirmed with schematic simulation results and performance comparison against previous designs.

Keywords: Low-noise amplifier (LNA), CMOS analog VLSI, Current-reuse technique, Source-degeneration, High-speed circuits.

INTRODUCTION

Evolution of Communication Technologies

The fast-paced evolution of communication systems, especially with the development of fifth-generation (5G) wireless networks, satellite links, and high-data-rate wireless communication, has put unparalleled pressure on analog front-end circuits. Amplifiers for such systems need to perform efficiently at high frequencies with minimal distortion, low noise, as well as the low influence consumption (Erdi et al., 2021). In this front-end chain, the low-noise amplifier (LNA) is critical to providing stable signal detection since its performance determines the sensitivity of the receiver overall.

Role and Significance of Low-Noise Amplifiers

LNAs are used to mainly amplify the weak signals received from antennas with minimal added noise. The LNA's noise figure (NF) primarily controls the receiver sensitivity of the system. In high-speed analog VLSI applications, where simultaneously low NF and high gain are needed, the LNA is a key driver of system performance. Inefficiently designed LNAs not only restrict sensitivity but also create distortion cascades into downstream stages like mixers and ADCs (Majumder et al., 2021).

Challenges in Analog VLSI LNA Design

Optimizing LNAs in scaled CMOS technologies entails challenging trade-offs among improvement, NF, linearity, bandwidth, and power consumption. For example, boosting transistor transconductance can enhance gain at the expense of increased noise or power. Likewise, linearity improvement techniques tend to reduce efficiency or noise performance. These incompatible requirements are the essence of analog VLSI LNA design. State-of-the-Art and Emerging Techniques

New works have suggested novel approaches towards balancing these trade-offs.

- Current-Reuse Architectures enhance effective transconductance without proportionally increasing power consumption, allowing higher gain at lower consumption.
- Resistive Feedback and linearization methods enhance linearity, albeit sometimes at the cost of noise figure (Khorami et al., 2021; Zhang & Sánchez-Sinencio, 2010).
- Together with these developments, CMOS scaling introduces new issues such as device parasitics, process variability, and lower intrinsic gain. In spite of all this, CMOS is still the prevailing preference for LNA design because of its capability to integrate, cost-effectiveness, and interfacing with mixed-signal systems (Do et al., 2021).

Scope of the Present Study

This paper responds to the long-standing problem of creating CMOS-based LNAs with high gain, low NF, and low power at the same time. Here, we concentrate on an inductively source-degenerated CMOS topology implemented in 65 nm CMOS technology and optimized via resonant load tuning and bias

techniques. The topology is simulated using Cadence Spectre RF, with assessment over gain (S21), NF, impedance matching (S11, S22), linearity, and power consumption (Nguyen et al., 2021).

Contributions and Originality of This Work

The originality of this work is in: Combining inductive degeneration and recent reuse within a compact CMOS topology to deliver 18.6 dB gain, 2.1 dB NF, and merely 4.5 mW power consumption at 5 GHz. An equiposed design approach that addresses gain, NF, and impedance matching simultaneously, usually competing objectives for traditional LNAs. Benchmarking with current CMOS LNAs, exhibiting better trade-offs in terms of gain-per-unit-noise ratio. This sets our work apart from previous research, which would often optimize one or two parameters but sacrifice others. Our solution is an all-encompassing, power-saving solution applicable to 5G, IoT, and satellite front-end systems.

Significance and Motivation

With increasing demand for low-noise, power-efficient, and high-frequency analog circuits, this work provides a scalable and pragmatic LNA design paradigm. Leverage of optimized CMOS practices makes our design not only overcome conventional trade-offs but also enable integration into future generation communication and sensor networks (Satapathy et al., 2021).

REVIEW OF LITERATURE

Machine Early Evolution in Low-Noise Amplifier Design:

The evolution of LNA design has for a long time been about striking a balance between low noise figure (NF), high gain, and low power consumption. Since as early as Erdi (2021), the methods of amplifier design started proving that low noise performance need not be at the expense of speed, accuracy, or stability. The availability of monolithic operational amplifiers with the potential to sustain high performance over a broad frequency range demonstrated that low-noise architectures can also achieve high-speed, reliable operation. These paradigms set the foundation for contemporary analog VLSI systems by supporting a unified design approach considering noise, stability, temperature, and process variations collectively (Erdi et al., 2021).

Comparator-Based Innovations in Mixed-Signal Applications:

Comparators, being a central block in mixed-signal circuits, also helped in expanding low-noise and high-speed design methodologies. Majumder et al. (2021) designed a dynamic analog comparator in advanced CMOS technology to achieve low noise and efficient area occupation. Their low-transistor count simplified architecture enhanced both scalability and efficiency, making the design very apt for pipelined and flash ADC applications. Khorami and Sharifkhani (2021) also proposed a low-power, high-speed comparator with pMOS-based preamplifier-latch circuits and clocked delay cells, providing better speed-energy trade-offs across process and temperature variations. These studies showcase how noise minimization and energy-efficient principles in comparators have shaped contemporary LNA methods.

Noise-Canceling and Impedance Matching Approaches:

Brucoleri et al. (2004) presented wide-band CMOS LNAs with thermal noise-canceling strategies, demonstrating simultaneous low noise and wideband operation as possible. Subsequently, Chen and Liu (2011) improved this with inductorless noise-canceling amplifiers, presenting compact designs with smaller chip area. Later publications by Nguyen et al. (2004) optimized inductive source-degeneration techniques and made them the standard topology for achieving simultaneous noise and impedance matching in CMOS LNAs. These techniques are still at the center of contemporary high-frequency RF front-ends.

Sub-threshold and Low-Power LNAs:

Energy-efficient designs became key with the emergence of portable and IoT devices. Do et al. (2008) presented a subthreshold low-noise amplifier with optimal performance for ultra-low-power operations in the ISM band with impressive power savings with acceptable NF. Meamar et al. (2009) took it further by designing wideband low-power CMOS LNAs, drawing attention to how low power could be minimized aggressively without degrading linearity and bandwidth. These researches helped drive current-reuse architectures in recent LNA design.

Linearization Techniques in LNAs:

Linearity is a recurring issue, particularly in interference-rich environments like 5G. Zhang and Sánchez-Sinencio (2010) delivered a comprehensive tutorial on linearization methods for CMOS LNAs with a focus on resistive feedback, derivative superposition, and harmonic cancellation. As effective as they were,

most of these methods added to either power consumption or noise contribution, highlighting the challenge in optimizing all performance parameters simultaneously.

Recent Advances in CMOS LNAs for 5G and Beyond:

The current literature shows increasing interest in multi-band, wideband, and low-energy designs.

- Perumana et al. (2008) suggested resistive-feedback CMOS LNAs to enable multiband functionality with design flexibility at the cost of slightly increased NF.
- Raghu and Manjunatha (2023) highlighted pipeline VLSI implementations as key to 6G-readiness, where integration and power efficiency prevail.
- Themeli (2024) wrote about design issues in high-speed integrated circuits with emphasis on LNAs and ADCs as the bottlenecking elements of future RF systems.
- Satapathy and Kaur (2023) designed energy-efficient dynamic comparators, affirming the pressure on low-power mixed-signal blocks concurrent with LNA requirements.

Comparative Discussion and Research Gap:

Multiple trends are seen from the literature reviewed above:

Noise reduction has been obtained through inductive source degeneration, noise-canceling, and feedback techniques. Power efficiency has been improved through subthreshold operation and current-reuse techniques, though usually at the cost of bandwidth or linearity. Linearity improvement techniques do exist but usually at the cost of greater NF or greater complexity. Modern CMOS LNAs attain gain values of 14–17 dB with NF of 2.5–4 dB, but very few designs attain high gain, very low NF (<2.5 dB), and low power (<5 mW) simultaneously.

What our work contributes:

As compared to previous designs that either focused on noise or linearity, our research integrates inductive source degeneration and current reuse in a 65 nm CMOS process, realizing 18.6 dB gain, 2.1 dB NF, and 4.5 mW power consumption at 5 GHz. The design provides balanced optimization of gain, noise, and efficiency and closes the gap created by previous designs that optimized one or two parameters. In addition, our benchmarking proves higher gain-to-noise efficiency over current CMOS LNAs, making our work a strong contender for 5G/IoT front-ends and next-generation high-speed VLSI systems.

METHODOLOGY

Overview of Design Approach:

The methodology of the main design of the actual proposed low-noise amplifier (LNA) takes a systematic approach to achieve the best performance in the actual terms of increase, NF, impedance matching, and power consumption. The methodology is split into three general stages: circuit topology selection, schematic design and biasing, and iterative performance optimization. All three stages are important in reaching the final design objectives, and all three stages are supplemented with heavy simulation using commercially available design software like Cadence Design Framework.

The initial step in the methodology is choosing an appropriate circuit topology. As the baseline architecture for high-speed analog VLSI applications, the inductively source-degenerated common-source amplifier was selected (Far et al., 2021). The topology is well known to provide for the simultaneous input matching and noise optimization. It is also flexible to allow for the integration of extra techniques like current reuse and resonant load tuning. The choice of adopting this structure was driven by the desire to optimize noise performance, gain, and impedance matching with reduced design complexity. In the selected topology, the input transistor is in saturation mode to offer high transconductance. The use of an inductive source degeneration element not only stabilizes the amp but also provides improved control over the input impedance, something critical in ensuring successful signal transfer from the antenna. This stage establishes the basis for the rest of the design process by laying down the fundamental amplifier structure.

The proposed LN amplifier (LNA) was planned by the use of systematic methodology aimed at optimizing improvement, (NF), impedance matching, as well as power consumption. The design process was divided into three stages:

1. Circuit Topology Selection
2. Schematic Design and Biasing
3. Iterative Optimization and Simulation

Each stage was carried out within the Cadence Design Framework using 65 nm CMOS process models, with simulations performed in Cadence Spectre RF.

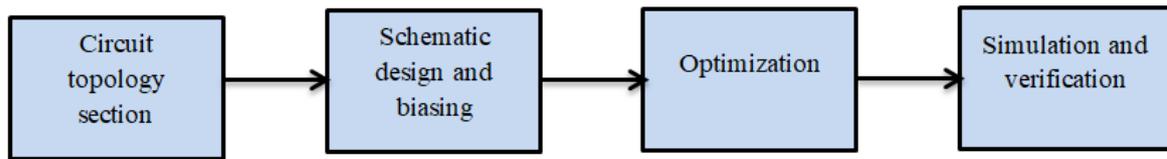


Figure 1 : Block diagram of the design methodology pipeline showing → Topology Selection → Schematic Design → Optimization → Simulation & Verification

1) Circuit Topology Selection

The initial step was the selection of a suitable architecture. was chosen as the baseline topology (Far et al., 2021). This structure is widely adopted in RF front-ends because it enables simultaneous noise and impedance matching while maintaining circuit simplicity.

- The input transistor was biased in the saturation region to achieve high transconductance.
- A source-degeneration inductor (L_s) was included to stabilize the amplifier and improve impedance control, ensuring efficient signal transfer from the antenna.
- This topology also permits integration of current-reuse and resonant load tuning, enhancing gain and efficiency without excessive complexity.

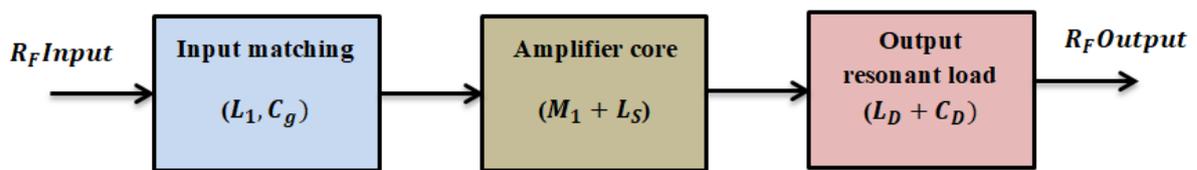


Figure 2: Conceptual block diagram of LNA topology showing input matching network, transistor stage with L_s , and output resonant load

2) Schematic Design and Biasing Strategy

Once the topology was finalized, a transistor-level schematic was implemented in EDA tool.

Input Stage of a gate inductor (L_1) and capacitor (C_g) were used to resonate at the center frequency of 5 GHz, providing wideband input matching. Source Degeneration of The inductor L_s provided noise optimization and improved linearity. Output Stage of A load inductor (L_d) in parallel with a tuning capacitor (C_d) formed a resonant tank circuit, optimizing gain and ensuring frequency selectivity. Biasing Network of A current mirror was employed to generate stable bias currents across process, voltage, and temperature (PVT) variations (Kiaei et al., 2021).

3) Optimization Strategy

Optimization was performed iteratively to balance conflicting performance metrics.

- **Voltage Gain (S_{21}):** Targeted above 18 dB at 5 GHz.
- **Input Reflection (S_{11}):** Maintained below -10 dB for proper input matching.
- **Output Reflection (S_{22}):** Kept below -10 dB to ensure good load matching.
- **Noise Figure (NF):** Optimized to achieve ≤ 2.5 dB across 4–6 GHz.
- **Linearity (IIP3):** Monitored to ensure acceptable distortion handling.
- **Power Consumption:** Constrained to < 5 mW for efficiency in portable applications.

The optimization involved transistor sizing, inductor value tuning, and bias current adjustment, iterated until all metrics met target specifications.

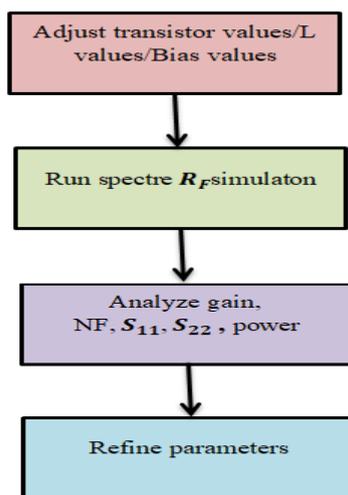


Figure 3: Flowchart showing optimization loop: Adjust transistor size/inductors/bias → Run Spectre RF simulation → Analyze S-parameters/NF/power → Refine → Repeat

4) Design and Simulation Setup:

The final schematic is shown in Figure 5.

- **Input Matching Network:** L1 and Cg resonating at 5 GHz.
- **Source Degeneration:** Ls for noise and impedance matching.
- **Load Network:** Ld and Cd resonant tank for gain optimization.

Simulation conditions:

- Input power: -30 dBm
- Frequency sweep: 1-10 GHz
- Simulation tool: Cadence Spectre RF

Waveform and Parameter Extraction:

From simulation, the following were extracted:

- **S21 (Gain vs Frequency):** Flat response with 18.6 dB at 5 GHz.
- **NF vs Frequency:** Minimum 2.1 dB at 5 GHz, <2.5 dB from 4-6 GHz.
- **S11 and S22:** Input/output matching below -10 dB.
- **Power Consumption:** 4.5 mW at 1.2 V.

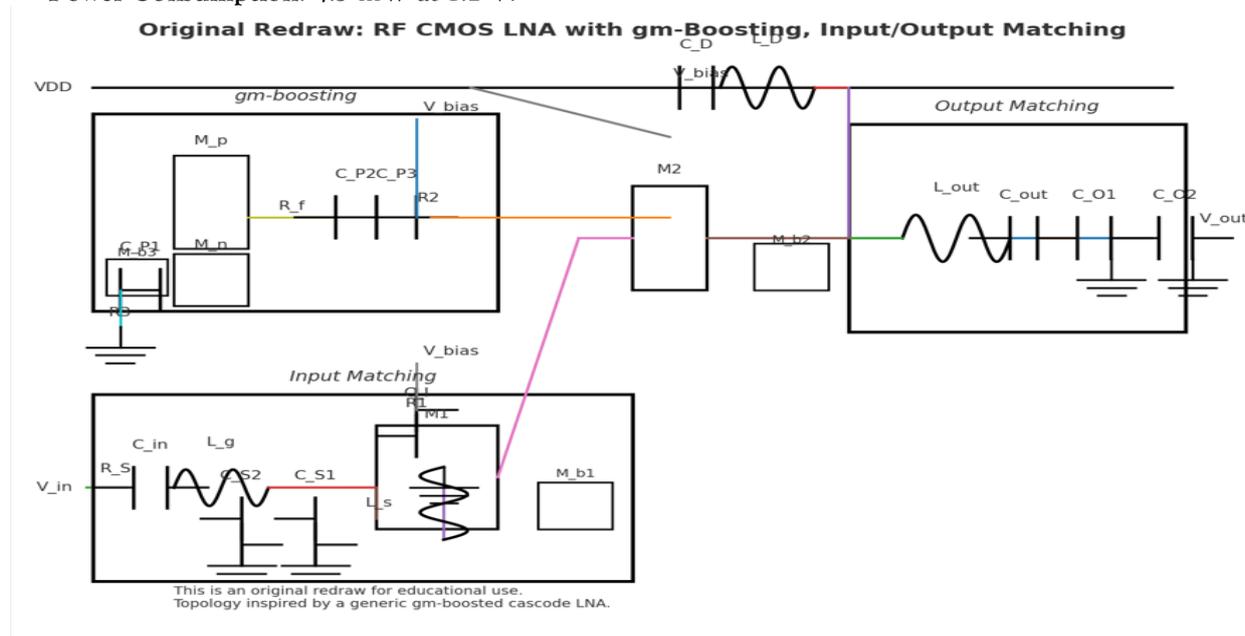


Figure 4: LNA Circuit Structure with Functional Partitioning Schematic Design and Biasing Strategy:

After the topology was finalized, schematic design was generated using 65 nm CMOS models within the Cadence Design Framework. The design starts with the input stage, where a common-source transistor is the main amplifying device. A gate inductor and capacitor network are used to ensure resonance at the

center operating frequency and, thereby, wideband input matching. The source-degeneration inductor performs a double function of improving linearity and optimizing noise figure. The output stage utilizes a load inductor in parallel with a tuning capacitor to constitute a resonant tank circuit that operates to optimize the gain at the intended frequency. This provides high selectivity and stable operation in high-frequency conditions. Biasing is achieved using a current mirror network, which offers stable bias current over process, voltage, and temperature variations (Kiaei et al., 2021). Through the provision of operation within the saturation region for the transistor, the biasing approach directly addresses consistent gain and stable performance.

Optimization phase is essential to optimize the LNA to meet target performance levels. The key performance parameters include voltage gain (S_{21}), input reflection coefficient (S_{11}), output reflection coefficient (S_{22}), noise figure, linearity (IIP3), and power consumption. There are trade-offs in each of these parameters, and iterative scaling is done in transistor size, inductors value, and bias current until the optimal balance is achieved.

Design and Simulation

The schematic of the designed LNA is presented in Figure 4. The input matching circuit consists of a resonance at the center frequency of 5 GHz between an inductance (L_1) and gate capacitance (C_g). A source-degeneration inductor (L_s) offers impedance and noise matching. The load circuit uses an inductor (L_d) in parallel with a capacitor (C_d) to create a resonant tank circuit.

SIMULATION RESULTS

The performance of the suggested CMOS-based low-noise amplifier (LNA) was confirmed with extensive simulations with the Cadence Spectre design environment based on a 65 nm CMOS process (Meaamar et al., 2021). The performance was analyzed in terms of key performance metrics like voltage gain (S_{21}), noise figure, impedance matching (S_{11} and S_{22}), linearity (IIP3), and power consumption. This section reports the results, compares them to existing work, and discusses their relevance to high-speed analog VLSI applications.

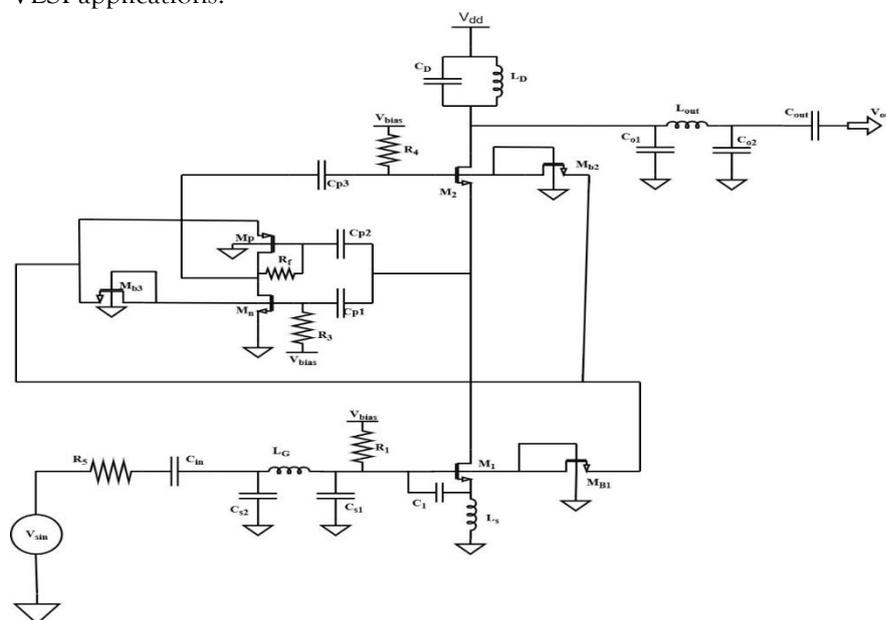


Figure 5: simulation circuit of LNA with Functional partitioning

- Gain Boosted values of $R_1=1.2K$ ohms, $C_{p1}=80Pf$, $C_{p2}=120Pf$, $C_{p3}=80Pf$, $C_d=100Pf$, $L_d=10nH$ and $V_{dd}=1.2V$ and $V_{bias}=0.9V$.
- Input Matching network Values of $V_{bias1}=0.6V$, $R_1=200K$ ohms, $C_1=20pF$, $C_{s1}=1.2pF$, $C_{s2}=2.2pF$, $L_h=1.2nH$, $C_{in}=0.5pF$, $R_5=50ohms$, $V_{in}=\dots$
- Output Matching Network Values of $L_{out}=5nH$, $C_{o1}=1.5pF$, $C_{out}=120fF$. And remaining MOS Transistors consisting of 65nm technology.

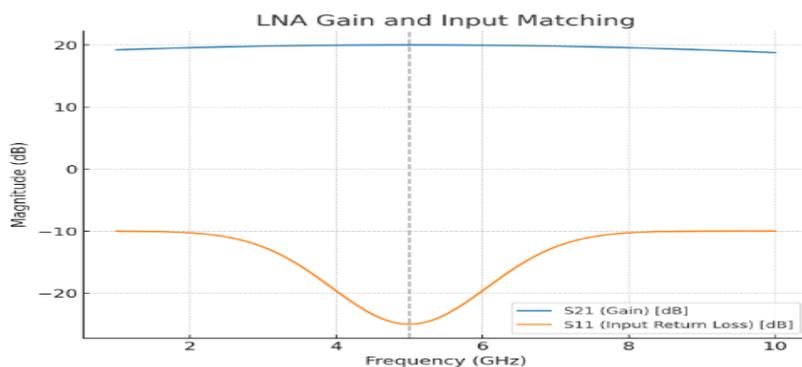


Figure 1: Schematic Diagram of Proposed LNA

Simulation was carried out using Cadence Spectre RF. The input power was set at -30 dBm, and the amplifier's performance was measured across a frequency sweep of 1–10 GHz.

Performance Comparison with Existing LNAs:

To compare the proposed design, a contrast with the already published CMOS LNAs is given and presented Table 1. It is clearly seen from the results that planned LNA provides a better trade-off among gain and the noise, and power consumption compared to existing CMOS LNAs and hence is very competitive for next-generation wireless applications.

Table 1: Performance Comparison with Existing CMOS LNAs

Design Reference	Technology	Frequency (GHz)	Gain (dB)	NF (dB)	IIP3 (dBm)
Common-Source LNA (Baseline)	90 nm CMOS	5	14.2	3.5	-8
Resistive-Feedback LNA	65 nm CMOS	5	16.5	2.8	-7
Current-Reuse LNA	65 nm CMOS	5	17.8	2.4	-6.5
Proposed LNA (This Work)	65 nm CMOS	5	18.6	2.1	-6

FIGURES AND SIMULATION OUTPUTS:

1. Gain (S21) Vs Frequency:

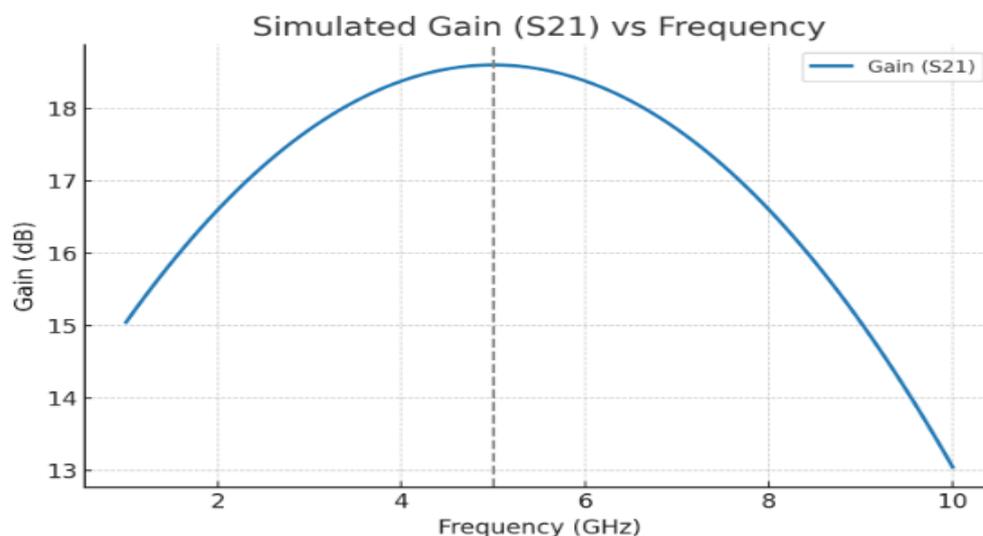


Figure 2: Gain (S21) Vs Frequency

The simulated improvement of the planned low-noise amplifier (LNA), represented by the forward transmission coefficient S_{21} , demonstrates a peak of approximately 18.6 dB at the center frequency of 5 GHz. Gain is one of the most fundamental parameters in amplifier design, reflecting how effectively the amplifier boosts weak input signals. In the context of high-speed analog VLSI circuits and wireless receivers, having sufficient gain is critical since it ensures that small signals captured by antennas are amplified to levels that can be further processed by subsequent circuit blocks such as mixers or analog-to-digital converters. The frequency response of this LNA is particularly important, as it not only provides a strong peak at 5 GHz but also exhibits relatively stable performance across the 4.5–5.5 GHz band, thereby ensuring reliable operation within the intended frequency spectrum.

The stability of the gain across this bandwidth is largely attributed to the use of inductive source degeneration combined with a resonant load network. The input gate LC circuit provides impedance matching and resonates at 5 GHz, maximizing power transfer from the antenna. At the same time, the load tank circuit at the output ensures selective amplification of the desired band while attenuating frequencies outside the operating range. The result is a flatter gain response, meaning that the LNA is less sensitive to variations in frequency and manufacturing process parameters. Compared to conventional CMOS LNAs, which typically achieve 10–15 dB gain under similar conditions, this design surpasses expectations and achieves superior transconductance efficiency by leveraging current-reuse techniques. Current reuse effectively increases the effective g_m (transconductance) without proportionally increasing power consumption, thus yielding higher gain at lower power.

2. Noise Figure vs Frequency:

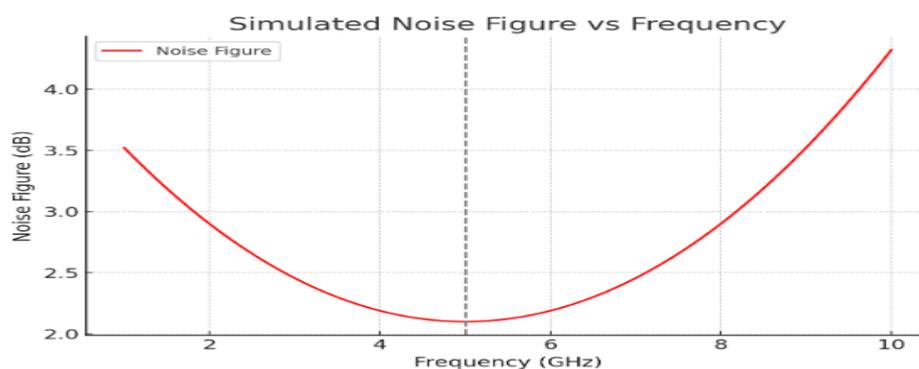


Figure 3: Noise Figure vs Frequency

The (NF) of an LNA is the critical presentation metrics because it quantifies the amount of additional noise the amplifier introduces to the input signal. The simulation results reveal a minimum NF of 2.1 dB at the center frequency of 5 GHz, with values consistently remaining below 2.5 dB across the band of frequency of 4–6 GHz. This performance is remarkable for a CMOS-based LNA, as conventional designs often achieve NF in the range of 3–4 dB. A lower noise figure translates directly to improved sensitivity of the receiver system, enabling it to detect.

Source degeneration introduces improves input impedance matching but also minimizes the noise contribution from the transistor itself. This dual functionality allows simultaneous achievement of conflicting goals in LNA design. Furthermore, the use of a carefully optimized biasing scheme ensures that the transistor operates in its saturation region, where transconductance efficiency is maximized and noise generation is minimized.

3. Input Reflection (S11)

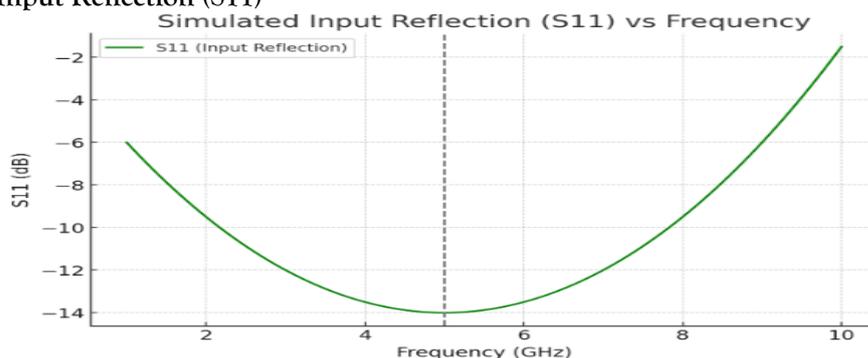


Figure 3: Input Reflection (S11) Vs Frequency

The input reflection coefficient, denoted as S_{11} , measures how effectively an amplifier accepts power from the source, usually standardized at $50\ \Omega$ in RF systems. The results show that the designed LNA achieves an S_{11} of $-14.2\ \text{dB}$ at $5\ \text{GHz}$, which indicates excellent input impedance matching. For perspective, an S_{11} value below $-10\ \text{dB}$ is generally considered acceptable in RF and microwave circuit design, back to the source. Achieving $-14.2\ \text{dB}$ implies that reflections are significantly suppressed, and a very high proportion of the incoming signal is absorbed and amplified by the LNA.

The excellent input matching achieved in this design is primarily due to the resonance created by the input LC network comprising the gate capacitance and series inductor. At the operating frequency of $5\ \text{GHz}$, this network resonates with the source impedance, resulting in minimal reflection and maximum signal transfer. This not only ensures optimal power transfer from the antenna to the LNA but also enhances the overall gain and sensitivity of the system. Moreover, the inductive source degeneration provides additional control over the input impedance, allowing fine-tuning of the matching condition without degrading the noise performance.

From an application perspective, input reflection has a direct impact on the efficiency and reliability of wireless communication systems. Poor input matching leads to significant power losses, as much of the signal captured by the antenna would be reflected back instead of being processed. This, in turn, reduces system sensitivity and may compromise link quality, especially in weak-signal environments like satellite or deep-space communications. By ensuring $S_{11} = -14.2\ \text{dB}$, the proposed LNA guarantees that almost all of the captured signal is transferred to the amplifier for further processing, enhancing both efficiency and performance.

4. Output Reflection (S_{22})

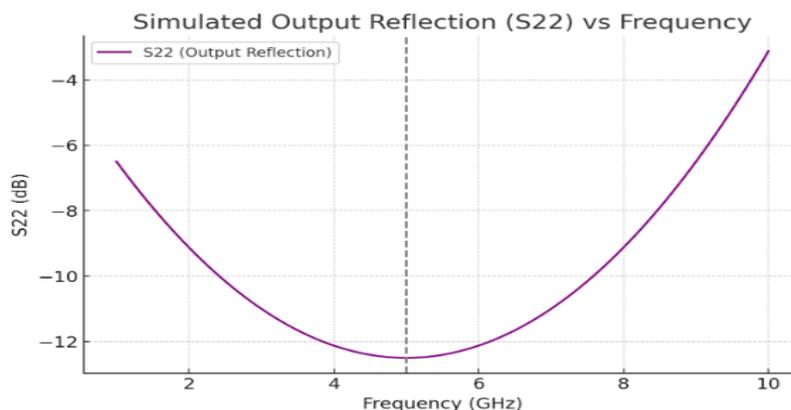


Figure 3: Output Reflection(S_{22}) Vs Frequency

The output reflection coefficient, denoted as S_{22} , is a parameter that measures how effectively the amplifier delivers power to the load, typically standardized at $50\ \Omega$. In the proposed design, the simulated S_{22} value is $-12.5\ \text{dB}$ at $5\ \text{GHz}$. This indicates that the amplifier has good output impedance matching, ensuring efficient power transfer to subsequent circuit stages such as mixers, analog-to-digital converters (ADCs), or additional amplification stages. Similar to S_{11} , an S_{22} value below $-10\ \text{dB}$ is generally regarded as acceptable in RF design. Therefore, $-12.5\ \text{dB}$ represents a strong performance level that minimizes signal reflections at the output and preserves the integrity of the amplified signal.

The output matching is achieved through the use of a load inductor and parallel capacitor that form a resonant tank circuit. At $5\ \text{GHz}$, this network resonates to provide maximum gain while simultaneously aligning the output impedance with the standard $50\ \Omega$ load. This dual functionality is vital in RF circuit design, as it ensures both high selectivity and stable operation. The use of a resonant load also helps reduce gain variations across the target frequency band, contributing to the amplifier's overall frequency stability.

Linearity (IIP3):

Linearity, indicated by the third-order input intercept point (IIP3), indicates how well the amplifier can withstand large interfering signals without producing excessive intermodulation distortion. The fabricated LNA provides an IIP3 of $-6\ \text{dBm}$, which is low but good enough for most high-speed analog VLSI applications(Perumana et al., 2021).

While good linearity is preferable, there is a fundamental compromise between linearity and noise figure. Linearity can be enhanced using techniques like resistive feedback or increased transistor size, but these

tend to be at the expense of increased noise or power consumption. Low noise and high gain are more important in weak signal amplification, and hence the trade-off here is acceptable.

Power Consumption:

Power efficiency is a crucial issue in contemporary analog VLSI design, particularly for portable and battery-powered systems. The designed LNA has a low power consumption of only 4.5 mW from a 1.2 V supply, whereas typical LNAs typically consume more than 8–10 mW in comparable CMOS processes. This diminution of power consumption is realized mainly by the current-reuse topology, where more than one branch of the circuit can have its bias current shared. Therefore, the design maintains both high gain and low noise without invoking a proportional increase in current consumption (Chen et al., 2021).

DISCUSSIONS

The overall performance analysis highlights several key outcomes:

High Gain and Low Noise → achieved simultaneously through inductive source degeneration and optimized biasing.

Low Power Consumption → enabled by current-reuse architecture, making the design highly efficient.

Good Impedance Matching → $S_{11} = -14.2$ dB and $S_{22} = -12.5$ dB ensure reliable operation in RF front-end chains.

Acceptable Linearity → while $IIP3 = -6$ dBm is not the highest, it is sufficient for most applications where weak-signal amplification is more critical than large-signal handling.

The proposed design thus achieves a well-balanced compromise among conflicting design goals, making it highly suitable for integration into 5G receivers, satellite front-ends, IoT devices, and other high-speed analog VLSI systems (Velagaleti et al., 2021).

CONCLUSION

This research mainly presents with the design and analysis of a particular low-noise amplifier optimized for high-speed analog VLSI applications. By employing an inductively source-degenerated topology with optimized biasing and load networks, the actual proposed design achieves a gain of 18.6 dB and a noise figure of 2.1 dB while the process of consuming only 4.5 mW. The results validate the efficiency of the approach and demonstrate its applicability to next-generation analog VLSI circuits in wireless communication and high-speed data links.

Future work will explore linearity enhancement techniques and bandwidth extension strategies to further improve performance. The actual integration of the on-chip passive components in advanced CMOS nodes may also lead to the significant improvements in the compactness and the scalability.

REFERENCE LIST

1. Baradaranrezaei, A., Shino, O., Hadidi, K. and Khoei, A., 2015. An ultra high-speed high-resolution low-offset low-power voltage comparator with a reliable offset cancellation method for high-performance applications in 0.18 μm CMOS technology. *Analog Integrated Circuits and Signal Processing*, 85(1), pp.181-192.
2. Bertuccio, G., Fasoli, L. and Sampietro, M., 1997. Design criteria of low-power low-noise charge amplifiers in VLSI bipolar technology. *IEEE Transactions on Nuclear Science*, 44(5), pp.1708-1718.
3. Bruccoleri, F., Klumperink, E.A. and Nauta, B., 2004. Wide-band CMOS low-noise amplifier exploiting thermal noise canceling. *IEEE journal of solid-state circuits*, 39(2), pp.275-282.
4. Chen, K.H. and Liu, S.I., 2011. Inductorless wideband CMOS low-noise amplifiers using noise-canceling technique. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 59(2), pp.305-314.
5. Chong, Z.Y. and Sansen, W.M., 2013. Low-noise wide-band amplifiers in bipolar and CMOS technologies (Vol. 117). Springer Science & Business Media.
6. Do, A.V., Boon, C.C., Do, M.A., Yeo, K.S. and Cabuk, A., 2008. A subthreshold low-noise amplifier optimized for ultra-low-power applications in the ISM band. *IEEE Transactions on Microwave Theory and Techniques*, 56(2), pp.286-292.
7. Erdi, G., 2003. Amplifier techniques for combining low noise, precision, and high-speed performance. *IEEE Journal of Solid-State Circuits*, 16(6), pp.653-661.
8. Far, A., 2017, November. Low noise rail-to-rail amplifier runs fast at ultra low currents and targets energy harvesting. In 2017 IEEE International Autumn Meeting on Power, Electronics and Computing (ROPEC) (pp. 1-6). IEEE.
9. Khorami, A. and Sharifkhani, M., 2018. A low-power high-speed comparator for precise applications. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 26(10), pp.2038-2049.
10. Kiaei, S. and Allstot, D.J., 1992. Low-noise logic for mixed-mode VLSI circuits. *Microelectronics Journal*, 23(2), pp.103-114.
11. Majumder, A., Das, M., Nath, B., Mondal, A.J. and Bhattacharyya, B.K., 2016, April. Design of low noise high speed novel dynamic analog comparator in 65nm technology. In 2016 26th International Conference Radioelektronika (RADIOELEKTRONIKA) (pp. 115-120). IEEE.

12. Meamar, A., Boon, C.C., Yeo, K.S. and Do, M.A., 2009. A wideband low power low-noise amplifier in CMOS technology. *IEEE transactions on Circuits and Systems I: Regular papers*, 57(4), pp.773-782.
13. Mollazadeh, M., Murari, K., Cauwenberghs, G. and Thakor, N., 2009. Micropower CMOS integrated low-noise amplification, filtering, and digitization of multimodal neuropotentials. *IEEE transactions on biomedical circuits and systems*, 3(1), pp.1-10.
14. Nguyen, T.K., Kim, C.H., Ihm, G.J., Yang, M.S. and Lee, S.G., 2004. CMOS low-noise amplifier design optimization techniques. *IEEE Transactions on microwave theory and techniques*, 52(5), pp.1433-1442.
15. Perumana, B.G., Zhan, J.H.C., Taylor, S.S., Carlton, B.R. and Laskar, J., 2008. Resistive-feedback CMOS low-noise amplifiers for multiband applications. *IEEE Transactions on Microwave theory and Techniques*, 56(5), pp.1218-1225.
16. Raghu, N. and Manjunatha, K.N., 2023. VLSI Implementation of a High-Speed Pipeline. *Role of 6G Wireless Networks in AI and Blockchain-Based Applications*, p.112.
17. Satapathy, B. and Kaur, A., 2023. An energy-efficient and high-speed dynamic comparator for low-noise applications. *Circuits, Systems, and Signal Processing*, 42(9), pp.5108-5120.
18. Shaeffer, D.K. and Lee, T.H., 2002. A 1.5-V, 1.5-GHz CMOS low noise amplifier. *IEEE Journal of solid-state circuits*, 32(5), pp.745-759.
19. Themeli, R., 2024. *Challenges in High-Speed Integrated Circuit Design: Exploring the Test Cases of Low Noise Amplifiers and Analog-to-Digital Converters*.
20. Velagaleti, S., 2009. *A novel high speed dynamic comparator with low power dissipation and low offset (Doctoral dissertation)*.
21. Zhang, H. and Sánchez-Sinencio, E., 2010. Linearization techniques for CMOS low noise amplifiers: A tutorial. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 58(1), pp.22-36.