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Performance-Driven Design of Two-Stage CMOS Op-Amp Using Bio-Inspired Dung Beetle Optimization Algorithm

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Abstract
As designer the task of sizing analog circuits has become more important due to complex trade-offs in CMOS analog design process. Power use, silicon size, unity-gain bandwidth, slew rate, and open-loop gain are just a few of the performance factors that need to be evaluated together. The problem is obviously multi-objective because there are so many design criteria. Transistor-level equations are used in traditional sizing methods, but these methods often don't find the best global solution because they rely on simplifying assumptions. Researchers have turned to metaheuristic optimization techniques to get around these problems. These techniques work well in design spaces that are very nonlinear. This paper investigates the implementation of the Dung Beetle Optimization (DBO) algorithm, a new bio-inspired approach was implemented for optimizing the circuit of CMOS two-stage operational amplifier of 130nm technology within the SPICE environment. The results show that DBO can lower the area and power use of transistors while still meeting design requirements. DBO consistently achieves more favorable trade-offs than other well-known evolutionary algorithms like Particle Swarm Optimization (PSO), Cuckoo Search (CS), Whale Optimization Algorithm (WOA) and Artificial Bee Colony (ABC). These results show that DBO is not only fast at searching, but also good at balancing conflicting design goals. This makes it a strong candidate for improving analog VLSI design automation.
Keywords: *CMOS VLSI Design, Op-Amp, Dung Beetle Optimization, Metaheuristics, Circuit Sizing*

1. INTRODUCTION

The development of modern electronics is closely linked to the advancement of analog and mixed-signal circuit technologies.[1] Despite digital circuitry is dominant in integrated systems, analog circuits play an equally critical role, serving as the interface between the physical world and digital processors.[2] Applications such as wireless communication, signal processing, automotive systems, industrial automation, biomedical instrumentation, and consumer electronics all rely heavily on high-performance analog building blocks. Among these, the operational amplifier (op-amp) remains a fundamental circuit, forming the basis of filters, data converters, oscillators, and control systems.[3]

Designing analog circuits in CMOS technology is significantly more challenging than digital design. Unlike digital circuits, which generally allow for automation due to predictable scaling behavior, analog circuits remain highly vulnerable to process variations and intricate device-level trade-offs. Key specifications such as bandwidth, power efficiency, slew rate, gain and chip area must be carefully optimized in tandem to satisfy performance goals. With the continued downscaling of CMOS technology, the incorporation of digital with analog circuit modules in a single chip becomes increasingly complex task. As a result, designing analog circuits by manually needs a lot of time and expects a lot of skill of the designers.[4], [5], [6]

To deal with these challenges, automation in circuit design has become a significant topic of research. Basically, analog design methodologies fall into two primary categories: knowledge-driven methods and optimization-driven methods. Knowledge-based methods generally rely on designer skills, rule sets, and mathematical calculations for transistor sizing. However they can be useful for comparatively basic designs but in case of advanced and complex circuits their dependency on assumptions generally limits their efficacy and resulting to inefficient solutions. In contrast, optimization-based methods define the design challenge as a mathematical optimization scenario, allowing advanced algorithms to meticulously explore and analyze the design space.[7], [8]
In analog circuit design, optimization strategies are often categorized into deterministic and metaheuristic techniques. Deterministic techniques can succeed well when the problem is precisely stated, but they are

generally constrained by their tendency to rely on particular solutions and their responsiveness to starting parameter selections. On the alternative hand, metaheuristic algorithms many of which took motivation from natural phenomena provide higher robustness by integrating dynamic exploration with a harmony between global and local search. Owing to their versatility and effectiveness, these algorithms are currently popular choices for dealing with the multidimensional, multi-objective, and extremely complex structure of analog design problems.[9], [10]

In recent years, bio-inspired metaheuristic approaches have attracted immense interest for resolving analog circuit design issues. Several methods, including Particle Swarm Optimization (PSO), Cuckoo Search (CS), Whale Optimization Algorithm (WOA) and Artificial Bee Colony (ABC), have showed success in optimizing circuit parameters. The Dung Beetle Optimization (DBO) algorithm has been presented as a unique approach that extends this line of research and delivers excellent global search performance while maintaining a solid balance between exploration and exploitation. [11] The approach uses inspiration from the natural habits of dung beetles, including strategies such as ball-rolling, navigation, and foraging for controlling the optimization process. [12]

The Dung Beetle Optimization (DBO) algorithm is used in this research to automatically create a two-stage CMOS operational amplifier. The technique is focused on optimizing essential design parameters while simultaneously minimizing power consumption and chip area. To test its performance, DBO is benchmarked against recognized optimization techniques such as PSO, ABC, WOA, and CS. The comparative analysis reveals that DBO delivers a more trustworthy and effective approach for analog circuit design automation, allowing enhanced control of complex trade-offs with higher accuracy and fewer dependencies on human intervention.[13]

2. Dung Beetle Optimizer

Nature has been a persistent source of motivation for metaheuristic optimization strategies. The Dung Beetle Optimizer (DBO) is one such approach, developed by replicating the unique behaviors of dung beetles in the natural environment. These insects demonstrate varied survival strategies—including rolling, dancing, reproducing, feeding, and stealing—that boost the flexibility and strength of the algorithm. By applying these characteristics, DBO maintains a good balance between global exploration of the search space and targeted local improvement, making it well-suited for difficult optimization tasks. Within the algorithm, the dung beetle population is broken down into subgroups—rollers, dancers, breeders, little beetles, and thieves—each governed by its own updating criteria. This category-based structure lowers the possibility of premature stagnation while increasing the rate of convergence.**[14]**

2.1Rolling Dung Beetles

Dung beetles are famous for their talent to make a circular ball from dung and roll down in straight lines. Certain beetles maintain straight trajectories by evaluating external references such as sun position or prevailing wind. DBO algorithm simulates this behavior by having each individual agents take a controlled step rather than a random walk. The step direction balances attraction to the current best solution with repulsion from the worst. This technique stimulates moving into desirable regions while steering out of areas associated with low fitness. This behavior is modeled in DBO as a position updating mechanism:

$$xi(t + 1) = xi(t) + \alpha \times k \times xi(t - 1) + b \times \Delta x \quad (1)$$

$$\Delta x = |xi(t) - Xworst| \quad (2)$$

Where

$xi(t)$: position of the ith beetle at iteration t

$\alpha \in \{-1,1\}$: natural coefficient

$k \in (0,0.2)$: deviation coefficient

$b \in (0,1)$: constant factor

$Xworst$: global worst position

2.2Dancing Beetles

When a rolling beetle encounters an obstacle in the straight path, it performs a unique dancing motion. This behaviour is used to reorient it's head and pick the new direction for identify an alternative straight path. In DBO algorithm this mechanism represents the redirection of the search process for shifting the

position when trapped in weak regions. Representing the changing angle with a formula adds diversity and helps the algorithm to escape from unfavorable region with enhanced exploration. In DBO, this is captured using a tangent-based update:

$$\mathbf{xi(t+1) = xi(t) + \tan(\theta) \mid xi(t) - xi(t-1) \mid} \quad (3)$$

Where:

$\boldsymbol{\theta \in [0, \pi]}$: random orientation angle

If $\boldsymbol{\theta = 0}$ or $\boldsymbol{\pi/2}$, the position remains unchanged. This mechanism introduces diversity by adjusting directions.

2.3Breeding Dung Beetles

Female dung beetles bury dung balls in secure places to protect their eggs, ensuring survival of their offspring. This behavior is abstracted in DBO as a boundary-based selection technique that refines the search region around promising solutions. It models the safe zone where future solutions (offspring) can be generated, ensuring the algorithm preserves quality while still exploring nearby possibilities.

$$\mathbf{xi(t+1) = X* + b1 \cdot (xi(t) - Lb*) + b2 \cdot (xi(t) - Ub*)} \quad (4)$$

Where:

$\mathbf{Lb* = max(X* \cdot (1 - R), Lb)}$, $\mathbf{Ub* = min(X* \cdot (1 + R), Ub)}$

$\mathbf{X*}$: current local best position

$\mathbf{R = 1 - tTmax}$: decay factor over iterations

$\mathbf{Lb, UbLb, Ub}$: global lower and upper bounds

$\mathbf{b1, b2}$: control parameters

This ensures a balance between exploration and exploitation.**[15]**

2.4Small Dung Beetles

Some beetles emerge to forage for food independently, representing scouting behavior. In DBO, small beetles are used to explore new regions of the solution space more widely. This allows the algorithm to avoid stagnation and keeps the diversity of the population intact. By defining foraging boundaries around the current best solution, the algorithm ensures both local improvement and global search capability. In DBO, this enhances global search ability:

$$\mathbf{xi(t+1) = xi(t) + C1 \cdot (xi(t) - Lbb) + C2 \cdot (xi(t) - Ubb)} \quad (5)$$

Where:

$\mathbf{Lbb = max(Xb \cdot (1 - R), Lb)}$, $\mathbf{Ubb = min(Xb \cdot (1 + R), Ub)}$

$\mathbf{Xb}$: global best position

$C1 \sim N(0,1)$: normally distributed random number

$C2 \in (0,1)$: random coefficient

This strategy diversifies the search process and prevents premature convergence.

2.5Thief Dung Beetles

A subset of dung beetles display stealing behavior, taking dung balls from others instead of creating their own. In optimization, this behavior is mapped to opportunistic exploitation of promising areas. Thief beetles adjust their positions by referencing both the best and locally optimal solutions, accelerating convergence toward high-quality regions while maintaining randomness to avoid being trapped. In DBO, this is modeled as:

$$\mathbf{xi(t+1) = Xb + S \cdot g \cdot (\mid xi(t) - X* \mid + \mid xi(t) - Xb \mid)} \quad (6)$$

Where:

S: constant scaling factor

$g \sim N(0,1)$: random Gaussian vector

Xb: global best position

$X*$: local best position

This enhances exploitation around the best regions found so far.

2.6 Application in This Work

Although DBO has been successfully applied in engineering optimization, image processing, and scheduling problems, its application to analog CMOS circuit design remains unexplored. In this research, DBO is employed for the first time to optimize the parameters of a two-stage CMOS operational amplifier

with a current mirror load. The population is divided into distinct beetle roles—rollers, breeders, small beetles, and thieves—mirroring their natural colony distribution. This structured search process enables efficient tuning of design variables such as transistor dimensions and biasing conditions, ultimately meeting performance objectives including gain, bandwidth, power consumption, and stability. In this work, DBO is applied for the automatic design of a two-stage CMOS operational amplifier, where the population size is set to 30. The groups are distributed as:6 rolling beetles,6 breeding beetles,7 small beetles,11 thief beetles. This setup confirms a well-adjusted optimization method for analog circuit design.

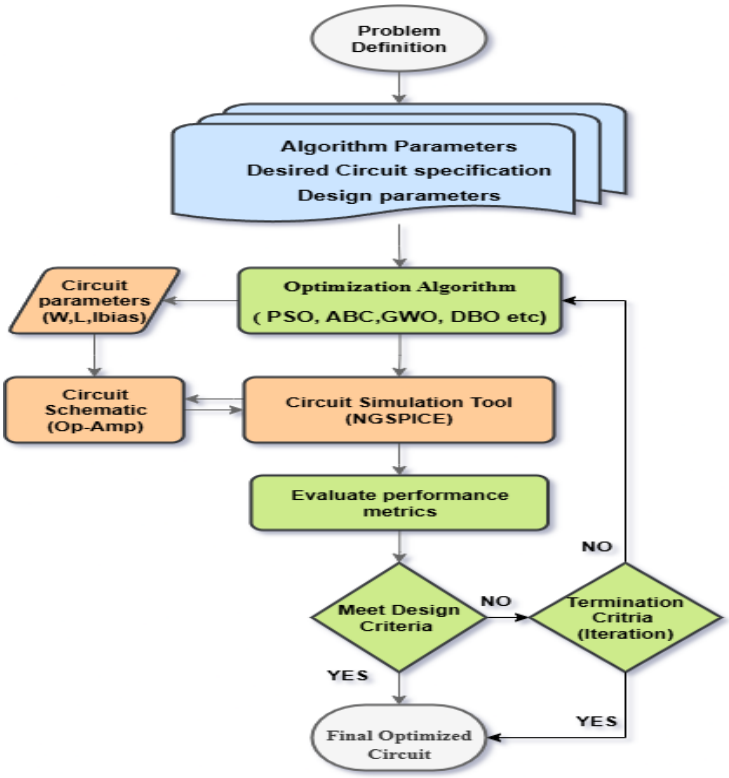

Figure 1. Workflow Diagram for Automatic Circuit Design

3. CMOS based two stage Operational Amplifier design criteria

The fundamental building block in analog and mixed-signal ICs is a two-stage CMOS operational amplifier. Op-amps are used throughout analog systems, including active filters, data converters (ADCs/DACs), sensor signal conditioning, power regulation/control loops, communications/baseband, and biomedical instrumentation. The design of two-stage CMOS op-amp must meet rigorous specifications. Designers must have balanced trade off between the circuit design parameters such as high gain, wide bandwidth, low power consumption, and stability. Achieve the complete set of design criteria while balancing the inherent trade-offs across the requirements is the complex task.**[16], [17]**

Designer commonly use the SPICE simulation for evaluation of performance of the design and apply the optimization algorithm such as DBO to achieve best solution by tunning device dimensions and bias current. **[18]**

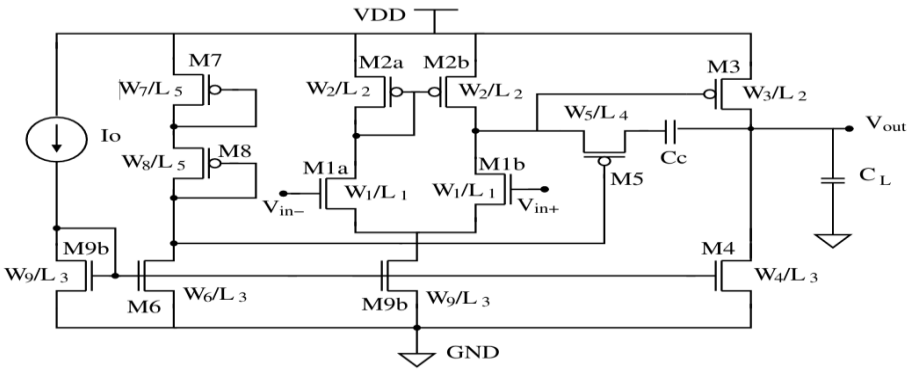

Figure 2. Circuit Design of two-stage Op-Amp

In CMOS based analog circuit design of two-stage operational amplifier designer have to take care of multiple interdependent specifications that are trade-off with each other. The amplifier's precision and operating speed is mainly express by the open-loop voltage gain (Av) and unity-gain bandwidth (UGB), whereas in shaping circuit's transient behavior and overall stability, the slew rate (SR) and phase margin (PM) play a major role. With these parameters the power supply rejection ratio (PSRR) and common-mode rejection ratio (CMRR) are also important to ensure resilience against external noise sources and help preserve signal quality. To achieve accurate results, feasible design considerations must include minimizing input offset, effective driving capacitive loads, and optimizing the output voltage swing. Together with these functional parameters of another important design priorities are minimum power dissipation (Pdiss) and smaller silicon area (TTA). These parameters are optimized by carefully tunning the transistor channel widths and lengths and adjusting bias currents so that the amplifier attain higher gain with stability and efficient in terms of power dissipation.**[19], [20]**

A conventional CMOS two-stage operational amplifier, shown in Figure 1,**[21]** is generally composed of a differential input pair with an active load, followed by a second gain stage. To maintain stability, a compensation capacitor is incorporated between the stages.**[22]** The behavior of this architecture has been investigated extensively using both analytical models and SPICE simulations. In the present study, the design is optimized under a supply voltage of ±1.2 V, driving a capacitive load of 0.5 pF, and implemented in a 0.13 µm CMOS technology.
Traditional manual tuning of transistor widths and lengths (W/L ratios) is not only time-consuming but also prone to suboptimal results due to the complexity of the design space. To address these challenges, metaheuristic optimization techniques are increasingly employed for analog circuit design. The circuit's performance is assessed using a fitness function.[23] To evaluate the design, a fitness function is established and computed using the data generated during circuit simulations.

$$F_{\varepsilon} = \sqrt{\sum \left(\frac{\text{Spec}_{\text{Desired}} - \text{Spec}_{\text{Sim}}}{\text{Spec}_{\text{Desired}}} \right)^2} \qquad (7)$$

In this work, the DBO algorithm is applied to automate the sizing of MOS transistors in a two-stage op-amp. The optimization framework links the algorithm with a circuit simulator, which evaluates the amplifier's performance for each candidate design. Target specifications such as voltage gain, unity-gain bandwidth, phase margin, and slew rate are predefined, and the algorithm searches for transistor dimensions that bring simulated values as close as possible to these targets.
This function quantifies the deviation between simulated results and target specifications. The optimization loop terminates when the error value becomes sufficiently small (less than 1×10^{-5}) or when the maximum iteration limit (100) is reached. Algorithm update the parameters and continue the search for the optimal result until the stop criteria is not achieved. By concerning this method, the DBO algorithm autonomously enhances the design of the CMOS two-stage op-amp and assures that the implemented configuration achieves the target specifications with nominal area and power dissipation.

4. Simulation Results And Discussions

In this study, Python language was used to program both the optimization and performance evaluation of a two-stage CMOS operational amplifier. All simulations were carried out on an Ubuntu 24.04 workstation running an Intel Core i5-8265U processor (1.60 GHz) with 8 GB of RAM. The design and verification tasks were performed using NGSPICE for a 0.13 µm CMOS process, operating at a ±1.2 V supply and driving a capacitive load of 0.5 pF. The main design goals included minimizing power consumption, enhancing amplifier gain, and reducing transistor area, while simultaneously satisfying critical specifications such as open-loop gain (Av), unity-gain bandwidth (UGB), phase margin (PM), slew rate (SR), common-mode rejection ratio (CMRR), power supply rejection ratio (PSRR), and output voltage swing.

As part of the optimization process, the sizing of all MOS transistors in the two-stage CMOS operational amplifier is carefully considered. The channel width (W) and channel length (L) of each device are treated as key design variables, since they have a direct impact on essential performance metrics such as voltage gain, bandwidth, output swing, and total power consumption.**[24], [25]** The input signal is processed through a differential amplifier formed by transistors M1a, M1b, M2a, M2b, along with the biasing device

M9. The subsequent gain stage is realized using transistors M3 and M4, while frequency stability is achieved through the compensation capacitor in conjunction with transistor M5. Adjusting the bias current in the amplifier can enhance voltage gain, but this improvement typically comes at the expense of bandwidth and slew rate. Similarly, the values of and the dimensions of M5 have a direct impact on phase margin and frequency response. Although lowering power consumption is desirable, it generally reduces the available slew rate.**[21]**

Hence, designing such an operational amplifier inevitably requires a careful balance between gain, bandwidth, stability, power efficiency, and transient performance. During optimization, the W/L ratios of all these devices are systematically varied within predefined upper and lower bounds, and the algorithm iteratively searches for the most efficient sizing combination that minimizes transistor area while satisfying performance requirements such as open-loop gain, phase margin, unity-gain bandwidth, and power consumption.**[26], [27]**

Table 1. Optimized design parameters for 0.13 µm CMOS two-stage op-amp

Sr. No.	Set of design variables	Range of design	Achieved values			
			ABC	PSO	HHO	DBO
1	W1 (µm)	0.5 to 10	0.61	0.50	1.25	0.50
2	W2 (µm)	0.5 to 10	3.85	0.50	1.09	10.00
3	W3 (µm)	0.5 to 10	0.57	4.78	2.72	0.96
4	W4 (µm)	0.5 to 10	9.68	8.35	3.69	2.04
5	W5 (µm)	0.5 to 10	3.57	10.00	2.05	0.80
6	W6 (µm)	0.5 to 10	2.18	0.50	0.76	0.50
7	W7 (µm)	0.5 to 10	6.92	10.00	0.50	10.00
8	W8 (µm)	0.5 to 10	0.50	0.50	0.58	0.50
9	W9 (µm)	0.5 to 10	7.32	5.70	2.98	2.47
10	L1 (µm)	0.2 to 1	0.43	0.35	0.37	0.35
11	L2 (µm)	0.2 to 1	0.39	0.31	0.35	0.37
12	L3 (µm)	0.2 to 1	0.51	0.75	0.28	0.63
13	L4 (µm)	0.2 to 1	0.20	0.20	0.23	0.20
14	L5 (µm)	0.2 to 1	0.86	1.00	0.31	1.00
15	I0 ((µA)	1 to 10	3.88	4.01	4.96	4.71
16	CC(pF)	0.001 to 1	0.65	0.21	0.25	0.00

The design of the 0.13 µm CMOS two-stage op-amp involves several key parameters that were optimized using different algorithms. The transistor widths (W1–W9) are considered in the range of 0.5 µm to 10 µm, while the lengths (L1–L5) are varied between 0.2 µm to 1 µm. In addition, the bias current (I0) is allowed within 1 µA to 10 µA, and the compensation capacitor (Cc) is tuned in the range of 0.001 pF to 1 pF. The optimized values for each parameter, as obtained through ABC, PSO, HHO, and DBO algorithms, are presented in Table 1. These results show how different optimization techniques determine suitable sizing and biasing conditions for achieving the desired amplifier performance.

Table 2. Desired performance criteria and obtained results for two-stage op-amp in 0.13 µm CMOS technology

Sr. No.	Specifications	Expected	Obtained Specification			
			ABC	PSO	HHO	DBO
1	***Av***(dB)	>40	76.45	74.77	75.80	79.84
2	PM (°)	>45	74.86	60.96	59.81	72.33
3	UGB (MHz)	>10	116.83	107.83	122.58	135.59
4	+ve PSSR (dB)	>40	76.67	90.86	83.78	84.81
5	CMRR (dB)	>70	80.71	73.93	78.28	92.86
6	***Pdiss***(µW)	<1000	34.84	34.97	20.88	34.84
7	RSR (V/µs)	>10	39.48	36.57	42.78	41.51
8	FSR (V/µs)	>10	28.93	28.73	37.61	29.17

9	TTA (μm2)	<200	24.39	29.83	6.38	23.55

The performance of the 0.13 μm CMOS two-stage op-amp was evaluated against standard design criteria using four optimization methods: ABC, PSO, HHO, and DBO. The specifications considered include open-loop gain, phase margin, unity gain bandwidth (UGB), positive power supply rejection ratio (+ve PSSR), common-mode rejection ratio (CMRR), power dissipation, slew rates (RSR and FSR), and total transistor area (TTA).

All algorithms satisfy the minimum requirements; however, DBO achieves the most favorable outcomes across critical parameters presented in Table 2. It provides the highest gain (79.84 dB) and largest UGB (135.59 MHz), both of which surpass the other methods. For CMRR, DBO achieves 92.86 dB, the best among all, demonstrating strong immunity to common-mode noise. The phase margin (72.33°) under DBO also remains well above the expected limit, ensuring stable operation. In terms of power, DBO maintains low dissipation (34.84 μW), comparable with ABC and PSO but slightly higher than HHO. The slew rate results indicate balanced performance, with DBO reaching 41.51 V/μs (RSR) and 29.17 V/μs (FSR), both exceeding the desired threshold. Additionally, DBO minimizes total transistor area (23.55 μm^2), making it more efficient than ABC and PSO, and close to HHO's compact design.

5. CONCLUSION

Analog CMOS circuit design is often time-consuming and requires iterative tuning, which motivates the use of intelligent optimization techniques. In this work, four evolutionary algorithms—ABC, PSO, HHO, and DBO—were applied for the automatic design of a two-stage CMOS op-amp in 0.13 μm technology using a simulation-based optimization framework. Among these methods, DBO consistently produced the best results, achieving the highest open-loop gain of 79.84 dB, a unity-gain bandwidth of 135.59 MHz, and a CMRR of 92.86 dB, while maintaining low power dissipation of 34.84 μW. These results indicate that DBO provides a more balanced trade-off between gain, bandwidth, and power efficiency compared to ABC, PSO, and HHO. Thus, the study confirms that DBO is the most effective optimization technique for automated analog circuit sizing, offering a compact, low-power, and high-performance solution for modern CMOS op-amp design.

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