International Journal of Environmental Sciences
ISSN: 2229-7359
Vol. 11 No. 20s, 2025
https://theaspd.com/index.php

A Digital Twin Of A Power Supply For Electrostatic Precipitators Designed In MATLAB/Simulink

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Abstract
Power supplies form a critical part of an electrostatic precipitator as it plays a crucial role in collection efficiency. Collection efficiency refers to the percentage of particulate matter removed from a gas stream as it passes through collecting plates. One problem associated with this power supply is a high voltage ripple that appears at the output of a transformer rectifier unit. To solve this problem a power supply that tends towards an idealistic peak to mean voltage ratio of unity is sought. The purpose of this study is to design a digital twin of a power supply for an electrostatic precipitator using MATLAB/Simulink software and analyze its performance. The characteristics of the output parameters of the transformer rectifier unit are obtained for a controlled firing angle. Its nominal data is presented where the performance of the model shows a peak to mean voltage ratio of 1.3. It is recommended to modify existing power supplies so that the voltage tends towards the idealistic peak to mean voltage ratio of unity to enhance collection efficiency.
Keywords : *Collection efficience, Voltage ripple, Transformer rectifier unit.*

1. INTRODUCTION

An Electrostatic Precipitator (ESP) is used to reduce environmental pollution / emissions. In an ESP, the particles of pollutants are electrically charged and pass through a strong electric field. The charged particles moving within a gas stream are therefore deflected towards collecting plates, to which they stick [1]. To create the ions that are required to charge the particles and to sustain the required strong electric field, high-voltage power supplies are required. The high value of DC voltage required ranges from 20 000 V to 100 000 V [2], to be supplied to the electrodes. Different topologies of power supplies exist which can be used to energize ESPs, which include the use of a single-phase thyristor-controlled power converter as a supply to a transformer rectifier unit (TRU) [3] [4] [5]. The control of a TRU's input voltage is achieved using a phase control method [6] [7], which inadvertently affects the ripple voltage on its output and subsequently heightens the peak-to-mean voltage ratio at certain firing delay angle. This problem lowers collection efficiency and prevents one from adhering to strict emission levels which are mandated by governments. Collection efficiency in an ESP requires a strong corona effect, which is explained by equation 1 [1].

$$\eta = 1 - e^{-k\bar{v}\tilde{V}} \quad (1)$$

Where k represents the ESP constant, $\bar{v}$ represent the mean voltage and $\tilde{V}$ represent the peak voltage respectively. To maximize the collection efficiency (η), the highest possible mean ($\bar{v}$) and peak ($\tilde{V}$) voltages are sought. However, flashovers occur at the peak voltage after reaching the limit of the dielectric breakdown voltage of the gas [8]. To prevent this, it requires that the power supply must exhibit a peak-to-mean voltage ratio of unity. These key parameters can be analyzed on a digital twin for a power supply unit. A digital twin of a power supply (PS) is a digital model of an intended or actual real-world physical product, system, or process (a physical twin) that serves as a digital counterpart of it for purposes such as simulation, integration, testing, monitoring, and maintenance [9]. It is primarily designed for data collection that can be used for decision making process of energy management and improving the collection efficiency of an ESP.

The purpose of this study is to design a digital twin for a power supply of an ESP using MATLAB/ Simulink software and analyze its performance in terms of the peak-to-mean voltage ratio. An overiew of an ESP is firstly given and then the digital twin is introduced. Simulation results are then provided followed by the conclusions.

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2. Power supply of an ESP

The traditional power supply unit (PSU) [10] of an ESP is shown in Figure 1. It is made up of three main components, the thyristor block, TRU block and the control block. The AC supply voltage from the local utility is fed into the thyristor block which is connected to the primary winding of the TRU through a current limiting reactor. The thyristor block comprises of two thyristors in anti-parallel (labelled as SCR stack in Figure 1) which are fired at specific points in the AC voltage wave form. The triggering is controlled by a firing angle control circuit. The TRU serves two main purposes, namely, to step up the low voltage of 525 V to 92 kV AC and to convert the high voltage AC to a maximum pulsating voltage peak of 130 kV. This voltage is applied to the electrodes of an ESP. The control block uses the feedback loop to measure and monitor parameters like voltage, and the processor controls the firing circuit (or firing delay angle) to optimize performance. The current limiting reactor is incorporated on the primary side of the TRU to protect the thyristor stack during flashovers/ sparking [11], an undesired phenomenon that occurs when the electrical field strength exceeds the breakdown voltage of the gas between the electrodes leading to a short circuit. On the secondary side of the TRU a high frequency (HF) reactor is incorporated to protect the rectifier and transformer from HF transient and high voltage spikes [12].

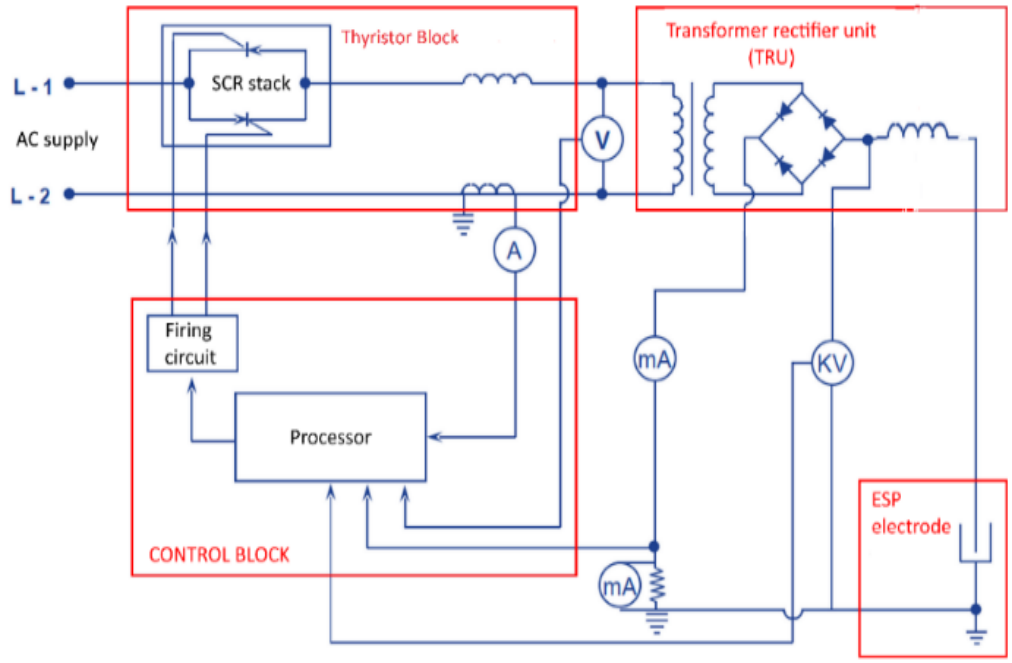

Figure 1: ESP power supply

3. A digital twin of the power supply for an ESP

A digital twin of power supply unit (PSU) shown in Figure 3 is designed in MATLAB/Simulink software. Its key components include the AC source, Thyristor stack, voltage controller, current limiting reactor, transformer rectifier unit TRU, high frequency HF choke, and ESP load which are modelled to form a power supply system. The following subsections explain its components in more detail.

3.1Thyristor block

Figure 2 shows the layout of the thyristor block, which includes the thyristor stack and firing control circuit. A thyristor stack is a semiconductor device that acts as a bi-directional switch, capable of controlling large amounts of AC power [13]. It is turned on or fired by a gate signal and will remain on until the current flowing through it drops below a certain threshold. The ellipse in Figure 2 highlights the thyristor stack. Snubber circuits are incorporated in the thyristor stack to protect the thyristors against overcurrent or overvoltage conditions. The thyristor firing circuit (note the components within the red rectangle), determines the firing delay angle (α) as commanded by the control input (labelled PID in Figure 2). With the control input being normalized, the firing delay angle is computed as, [14].

$$\alpha = \cos^{-1}(2 \cdot \text{PID} - 1) \quad (2)$$

The firing delay starts from the zero crossings of the supply voltage and hence requires synchronisation. This is achieved by the last components in the firing circuit block.

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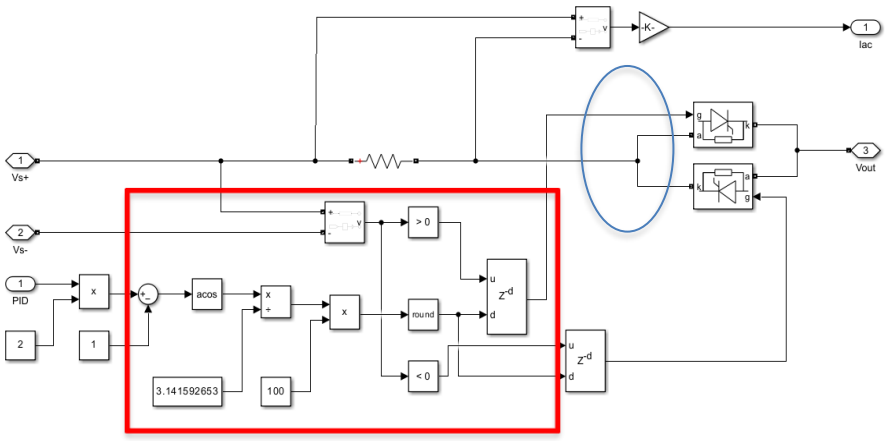

Figure 2: Thyristor and firing circuit

3.2The control block

The layout of the entire digital twin is shown in Figure 3. The thyristor block (upper left block) was discussed in the previous section. The control block (in the shaded rectangle) consists of a feedback loop and a Proportional-Integral-Derivative (PID) controller [15].

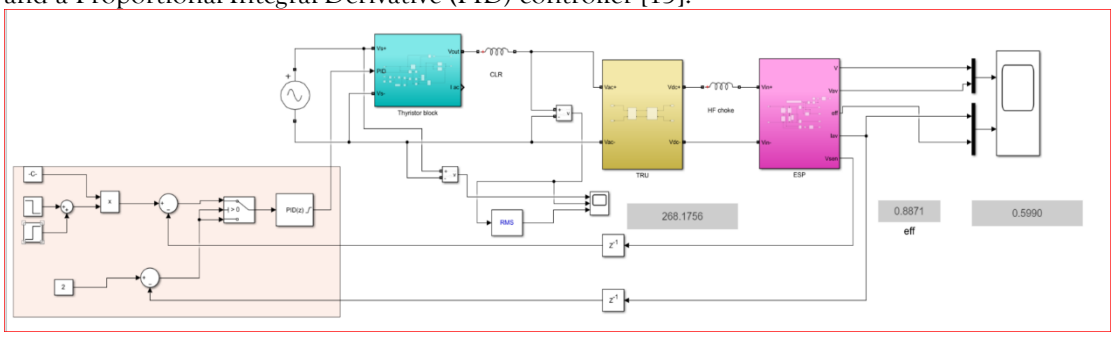

Figure 3: The digital twin from MATLAB

In the feedback loop, the output voltage and current parameters from an ESP are inputs to the controller. The main objective of the PID controller is to secure a constant output voltage for possible disturbances and different operational conditions. The PID controller commands the firing control circuit/block based on the output error of the feedback loop system. It consists of the proportional (Kp), integral (Ki), and derivative (Kd), parameters that determine: (i) the reaction to the current error, (ii) the reaction based on sum of recent errors and (iii) the reaction to the rate at which the error has been changing. To achieve optimal system performance, these parameters can be tuned as they feature in equation 3 [16] [17].

$$u(t) = K_p e(t) + K_i \int_0^t e(t) + K_d \frac{de(t)}{dt} \quad (3)$$

3.3Current limiting reactor

A current limiter reactor (CLR) is incorporated between the thyristor block and the TRU to limit fault currents (see Figure 3). It protects them when ESP flashovers occur, and thus from extreme current peaks [18]. It also helps to smooth the current waveforms on the TRU input [19]. It can be considered a two-leg iron core choke coil with a significant air gap [20]. Its inductive reactance is typically 3 % to 5 % lower than the total impedance of the circuit.

3.4The transformer-rectifier unit

Figure 4 shows the transformer-rectifier unit (TRU) (the middle block in figure 3), it is a step-up transformer connected to the bridge rectifier circuit. The two components making up a TRU are explained.

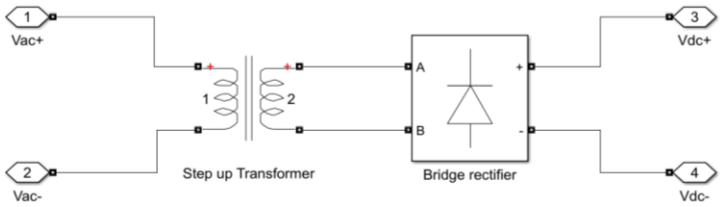

Figure 4: TRU

The high voltage (HV) rectifier diode comprises a series of cascaded diodes in each leg. The series of cascaded diodes must be capable of blocking at least twice the peak output voltage of the TRU set [21]. The step-up transformer is characterized by the turns ratio (n) and the inductive reactance under short circuit conditions (XLsc). The turns ratio (n) of the TRU is typically designed at about 1.05 to 1.1 times greater than the rated ratio [20]. The value of XLsc is between 25 % and 40 % of the TRU impedance, to reduce the current surges between 2.9 and 2.5 times [1]. One way to increase the XLsc is by expanding the space between the coil sections to increase the leakage inductance [22]. This procedure leads to an appropriate insulating structure that endures relatively high voltage spikes [22]. However, the transformer losses, size, and weight will be increased by higher leakage inductance [23]. Another way to increase the XLsc is by employing the CLR as a separate external inductance to achieve the desired amount [24]. Specifying the ESP ratings as $V_{DC\,(max)}$ = 83kV and $I_{DC(avg)}$ = 800 mA, allows for calculating all the essential quantities of the TRU:

$$V_{peak\,(sec)} = \frac{V_{DC} \times \pi}{2} = \frac{83kV \times \pi}{2} = 130kV \quad (4)$$

$$V_{RMS\,(sec)} = \frac{V_p}{\sqrt{2}} = 92kV \quad (5)$$

$$FF = \frac{V_{RMS}}{V_{DC}} = 1.11$$

Table 1 summarizes the parameters of the step-up transformer and bridge rectifier circuits that include the rated power of 104 kVA, I_{RMS} 1120 mA and I peak 1585 mA of the TRU.

Table 1: TRU HV rectifier parameters

Parameters	Rating
V primary	525 V
I Primary	198 A
Rated power	104 kVA
I DC average	800 mA
I sec-RMS	1120 mA
V secondary	92 kV
V peak	130 kV
I peak	1585 mA

3.5 High frequency choke

The high-frequency (HF) choke is an air-core inductor (ACI) that is connected between the TRU and ESP (see Figure 3). The transient high voltage spikes and disturbances caused by the sparking ESP are like an HF oscillation of a few MHz [25]. The HF choke protects the rectifier and transformer from HF transient high voltage spikes [12]. Typically, the HF chokes is rated at 70.6 mH and must withstand up to 2 times the peak rated voltage.

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3.6The electrostatic precipitator load

Figure 5 depicts the load of an ESP (right block in Figure 3); it is represented by a resistor (R4) of 95 kΩ [21]connected in parallel with a capacitor (C2) of 210 nF [26]. The collection efficiency equation (1) is incorporated into the model (see top-right block of Figure 5). Measuring the voltage on the HV side requires two resistors in series (creating a voltage divider circuit made up of R2 (10 MΩ) and R3 (148.9 Ω). The average current (IDC-Avg) of the TRU is 800 mA and is measured by the shunt resistor (R1) with a value of 1 kΩ.

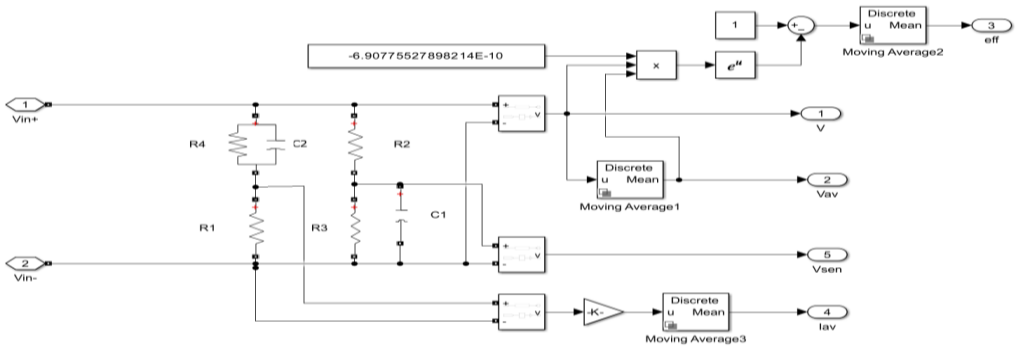

Figure 5: Representation of the load of an ESP

4. RESULTS AND DISCUSSION

The results of a digital twin of a power supply for an ESP are presented. The voltage peak and mean voltage parameters are analysed with an intention to improve the collection efficiency and energy management without causing flashovers. Two sets of results are shown. The first set shows the source voltage (shown in blue) and TRU input voltage (shown in orange). The second set is the TRU output, showing the peak voltage and mean voltage.

4.1Source voltage and thyristor block results

Figure 6 shows the source voltage at a frequency of 50 Hz with a peak voltage of 742.46 V. The control is set to 68% and the resulting firing delay angle (α) is calculated using equation 2 to be α = 68°. The output voltage of the thyristor stack shows an RMS measured voltage of approximately 268.1756 V, this can also be determined theoretically by equation 6.

$$Vrms = \sqrt{\frac{Vm^2}{\pi} \int_{\alpha}^{\pi} (\sin(\theta))^2 \, d\theta} \qquad (6)$$

It can also be noted that the shape of the output voltage of the thyristor stack is distorted due to the switching effect. To test the system response, the control is stepped down to 0 % @ 100 ms and stepped up 68 % @ 150 ms. The RMS voltage drop from 268.1756 V to 0 V within 20 ms.

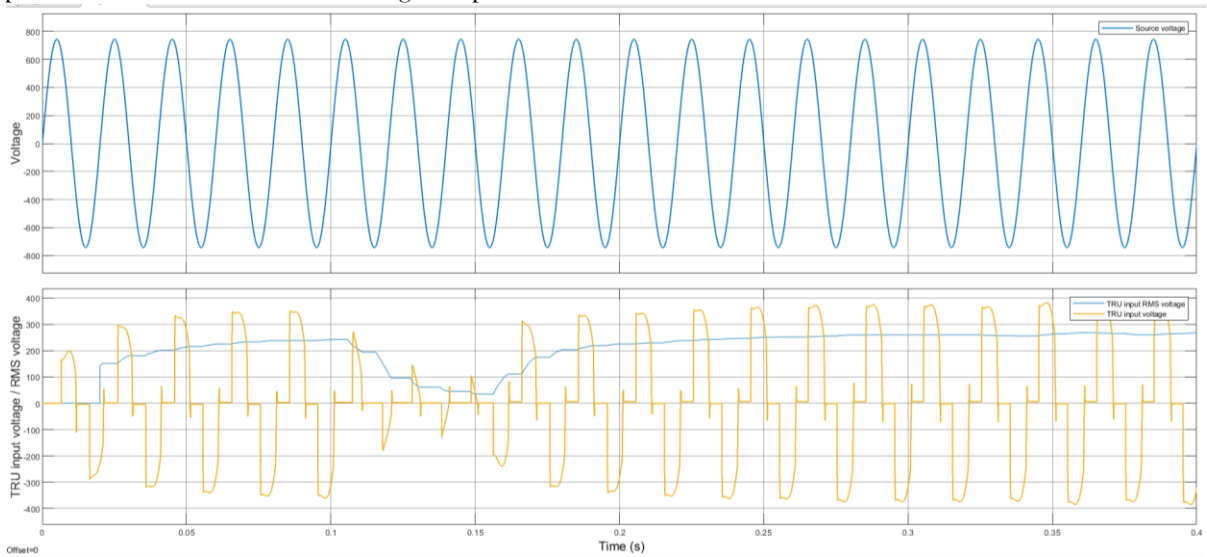

Figure 6: Supply voltage and TRU input voltage

4.2Output of the TRU

Figure 7 shows the output of the TRU, first picture is the output voltages. The second picture showing the collection efficiency and DC average current. In the first picture the peak voltage (blue wave) can be seen to be 70 kV, and the mean voltage (orange wave) is 53 kV. The peak to mean voltage ratio is then calculated to be 1.3. In the second picture, with the control voltage at 68 %, the collection efficiency (blue) is at 90 % at average current (yellow) 599 mA for the major duration of the time. During the time interval between 100 ms and 150 ms, when the control is stepped down to 0 %. The voltage waveform decreases and increases gradually due to the capacitive nature of an ESP. The current response is relatively fast, i.e. returning to 0 A within 20 ms (one 50 Hz cycle).

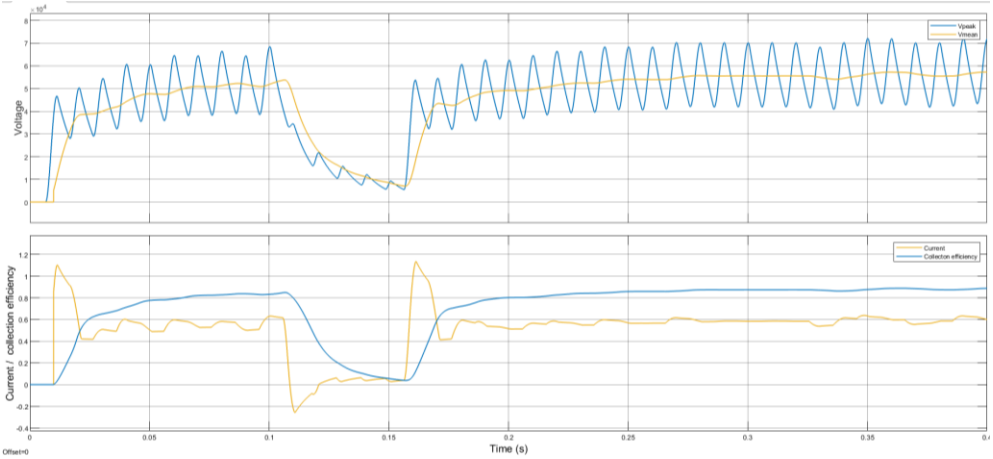

Figure 7: Secondary side of the TRU

Figure 8 shows the output voltage of a real-world ESP. The voltage can be seen to have a peak voltage of 70 kV (the legend on the top right indicates kV), and an average DC voltage of 52 kV (black dotted line). This agrees remarkably well with the simulation result shown in the previous figure.

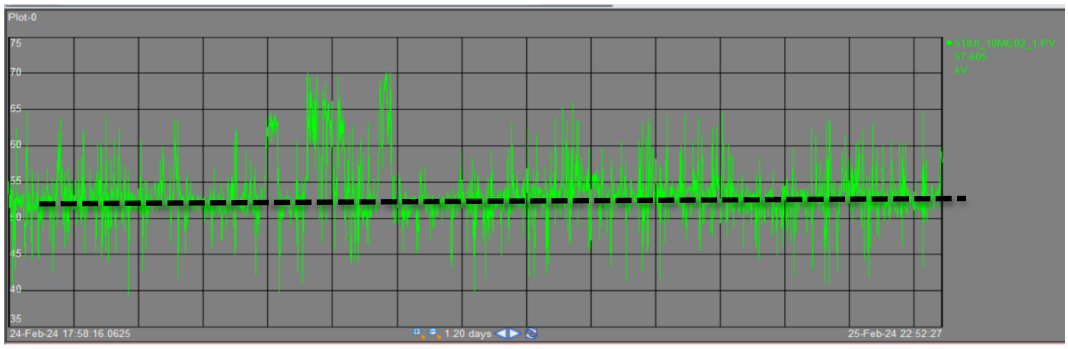

Figure 8: Output voltage of a real word ESP

5. CONCLUSIONS

The purpose of this study was to design a digital twin of a power supply for an ESP to analyze its performance. This was successfully achieved using MATLAB/Simulink software. Its performance data was compared with the power supply of a real-world ESP where both revealed a peak voltage of 70 kV and a mean voltage of 52/3 kV. This equates to a peak to mean voltage ratio of 1.3. This key observation implies that the real-world power supply will yield a low collection efficiency. The following challenges characterises the power supply: the phase control at the input of the TRU is inevitably distorting the input voltage source; the control response is sluggish, responding in 20 ms when stepped down to 0 %, which could lead to electrode damage during flash-over. It is therefore recommended to consider merging topologies to improve the collection efficiency. This efficiency may also be improved by retrofitting an existing power supply where the control strategy is modified, or by incorporating a low pass filter and elevating the input frequency to achieve a peak to mean voltage ratio of unity, or by increasing the response time of the control system.

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