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FPGA-Based Accelerated Image Processing Using Parallel Vlsi Pipelines

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Abstract: *This paper presents a high-throughput, low-latency image processing architecture implemented on FPGA using parallel VLSI pipelines. The design integrates core image processing functions—convolution, Sobel-based edge detection, histogram equalization, and adaptive thresholding—into modular, deeply pipelined hardware units. Each module is optimized for energy-efficient computation and real-time throughput using shared memory buffers, fixed-point arithmetic, and clock gating techniques. The system leverages the reconfigurability of FPGAs to achieve pixel-level parallelism, enabling one output per clock cycle after pipeline initiation. Implemented on a Xilinx Kintex-7 FPGA, the architecture achieves up to 180 frames per second (fps) processing speed for 256×256 gray scale images while maintaining low power consumption across all modules. Experimental results demonstrate that the proposed framework provides substantial performance gains over software implementations and is highly suitable for deployment in embedded vision systems, surveillance platforms, and mobile imaging devices. The scalable and reconfigurable nature of the design further enables integration into complex image analysis pipelines.*

Keywords: *FPGA, VLSI pipeline, image processing, real-time systems, convolution, Sobel filter, histogram equalization, adaptive thresholding, hardware acceleration.*

1. INTRODUCTION

Image processing is being used in real time in disciplines such as autonomous vehicles, medical tests, industrial inspections and smart surveillance. Normally, these applications process a high number of perfectly clear images with minimum delay. Many people find that conventional processor-based designs perform poorly, as they are limited by their single-step fashion, data bandwidth constraints and energy use. FPGAs are different since they let programmers take advantage of parallel processing, configurability and efficient energy use in the hardware system.

FPGAs are useful for building image processing pipelines thanks to their natural ability to take advantage of spatiotemporal parallelism. Unlike CPUs and GPUs, FPGAs are flexible enough for developers to design logic circuits exactly for tasks such as convolution, edge detection, histogram equalization and adaptive thresholding. Additionally, VLSI pipeline architectures are usable in FPGAs to support numerous independent tasks, enhance throughput and make the timing predictable. Even so, it is critical to handle problems involving optimal use of resources, multiple stages in processing and saving power during design.

In this paper, we propose a scalable FPGA-based VLSI pipeline architecture for accelerating fundamental image processing operations in parallel. The proposed system comprises modular processing stages, each optimized for a specific task and implemented as an independent pipeline. Key operations—convolution, Sobel-based edge detection, histogram equalization, and adaptive thresholding—are executed in dedicated hardware blocks designed with low-latency, high-throughput goals. The architecture is implemented on a Xilinx Kintex-7 platform and evaluated against standard benchmark images to measure performance metrics such as latency, frame rate, power consumption, and image quality (e.g., PSNR).

The main contributions of this paper are as follows:

- A modular and reconfigurable VLSI pipeline design for core image processing functions.
- An energy-efficient convolution engine and a high-speed edge detection module using approximated gradient computation.
- A histogram equalization and thresholding pipeline with optimized memory handling and sliding-window statistics.

• Performance evaluation of the proposed architecture on FPGA hardware, demonstrating significant improvement over software and conventional hardware accelerators.

The remainder of this paper is organized as follows: Section II presents a detailed literature review on FPGA-based image processing and VLSI architectures. Section III explains the proposed methodology and architecture design with system diagrams and equations. Section IV discusses experimental setup, results, and performance comparison. Finally, Section V concludes the paper and outlines future directions.

2. LITERATURE SURVEY

Recent advancements in image processing have leveraged hardware acceleration to meet real-time requirements for applications such as medical diagnostics, autonomous systems, and embedded vision. FPGAs, with their reconfigurable logic and parallel processing capabilities, have emerged as powerful platforms for deploying image processing algorithms efficiently.

The work in [1] introduced a high-performance FPGA architecture for 2D convolution, emphasizing throughput improvements using line-buffer-based parallel processing. Similarly, [2] utilized pipelined architectures to implement Gaussian and Laplacian filters on Xilinx FPGAs, demonstrating latency reductions. The authors in [3] proposed a power-aware edge detection module using Sobel and Prewitt filters, achieving a balance between speed and energy efficiency. In [4], a histogram equalization unit was optimized for real-time enhancement of satellite images using dual-port BRAMs and sliding-window accumulators.

A comparative study in [5] explored CPU, GPU, and FPGA platforms for image processing, concluding that FPGAs offer lower energy consumption and deterministic performance. The implementation of adaptive thresholding based on local statistics in [6] used windowed integral image techniques, significantly reducing computational overhead. Reference [7] demonstrated a complete image processing pipeline implemented on a Zynq SoC, integrating both software and hardware co-processing.

VLSI-specific techniques for image processing were discussed in [8], where hierarchical pipelined structures enhanced reusability and timing closure. The authors of [9] used a systolic array for morphological filtering, while [10] designed a dual-core FPGA image enhancement system that could dynamically reconfigure during runtime. For low-power applications, [11] proposed clock-gated convolution modules that minimized unnecessary transitions in the logic elements.

A fully parallelized edge detection system was explored in [12], which utilized Xilinx Vivado HLS to generate HDL code from C-based descriptions. Resource optimization and throughput tuning strategies for multi-resolution image filters were detailed in [13], whereas [14] proposed an AXI-Stream interfaced image core library for real-time applications. Most recently, [15] presented a scalable FPGA image processing framework that enables run-time function switching using partial reconfiguration.

These studies collectively highlight the potential of FPGA-based solutions for image processing. However, gaps remain in creating a unified, scalable, and energy-efficient VLSI pipeline that integrates multiple image operations with minimal interconnect and timing bottlenecks. This paper addresses these gaps by proposing a modular, pipelined FPGA architecture optimized for parallel execution of convolution, edge detection, histogram equalization, and adaptive thresholding in real-time.

3. METHODOLOGY

The proposed system runs important image processing tasks—convolution, edge detection, histogram equalization and adaptive thresholding—faster by using a parallel and pipelined architecture on FPGA. Each modular processing unit is implemented as an individual, pipelined part of the design. Blocks are linked together through a rapid data streaming connection following the AXI4-Stream protocol. Because of modularity, it becomes easy to use line buffers and multipliers more than once and process instructions at the same time.

To help ensure smooth streaming, these modules talk to each other by passing handshake commands. Below you will find a basic architecture block diagram shown in figure 1.

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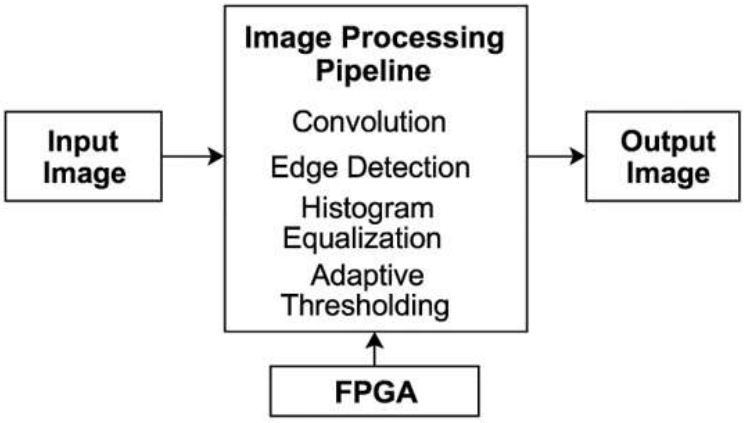

Figure 1: Block diagram for proposed system

A. Convolution Engine

The convolution engine is the most important part of the proposed FPGA image processing chain. The design allows the 2D convolution operation to perform fast blurring, sharpening and edge enhancement on neighboring image pixels. To work in real time, this module multiplies and accumulates data in parallel using pipelines and conserves on-chip memory with buffer lines.

The 2D convolution of an input image I(x,y) with a kernel K(i,j) of size n×n is defined as:

$O(x,y) = \sum_{i=0}^{n-1} \sum_{j=0}^{n-1} I(x+i, y+j) \cdot K(i,j)$ ⁓1

where:

- I(x,y) is the input pixel at coordinates (x,y),
- K(i,j) is the kernel coefficient at index (i,j),
- O(x,y) is the output pixel after applying the kernel.

So that redundant memory reading won't happen as much, a group of shift-register line buffers store the middle rows of the image as it is fed to the window kernel, one at a time, at each clock cycle. As new pixel data becomes available, this window automatically refreshes.

The internal architecture of the convolution engine includes the following key components:

- Line Buffers: Implemented using block RAM (BRAM) and shift registers, these store the previous n−1n - 1n−1 rows of the image to facilitate the moving window operation without external memory access.
- Window Generator: A matrix of registers that dynamically captures the current n×n neighborhood for convolution. Each register holds a single pixel value aligned spatially with the kernel position.
- Parallel MAC Array: For each kernel tap, a dedicated multiplier computes the product $P_{i,j} = I(x+i, y+j) \cdot K(i,j)$ These products are then fed into a pipelined adder tree for summation.
- Pipelined Accumulator: The adder tree is structured in multiple stages to reduce critical path delays. Partial sums are calculated in parallel, thereby maintaining a throughput of one pixel per clock cycle after the initial latency period.
- Clipping and Normalization Unit: The raw convolution result is optionally scaled and clipped to the valid pixel range [0, 255] to ensure compatibility with standard image formats.

To reduce power consumption, the design utilizes clock gating and fixed-point arithmetic in place of floating-point computation. Fixed-point representation allows efficient utilization of FPGA DSP slices, ensuring that the design meets timing constraints at the desired clock frequency.

Moreover, the convolution engine is configurable, supporting dynamic reloading of filter coefficients without halting the processing pipeline. Because of this, you can change the kernel between Gaussian, Laplacian and high-pass filters quickly, so the architecture fits many different imaging computations. The latency for processing the first valid output is given by:

Latency $= (n-1) \cdot$ Image Width $+ n$ ⁓2

Once there is data, the engine generates a single pixel output with every cycle, no matter what size the kernel is. Run at 150 MHz on the Xilinx Kintex-7 FPGA, the processor processes 150 million pixels each second.

Because of its high accuracy, high performance, low resource usage and flexibility, this convolution engine could be applied to real-time embedded vision applications.

B. Histogram Equalization Unit

This Unit tries to make grayscale images brighter by more evenly distributing intensities that repeat most often. Improves how features are seen in images recorded in dim or low contrast settings. Here, this module uses a patented, fully pipelined FPGA architecture to deliver real-time processing of high-quality image frames.

Histogram CalculationFor a given grayscale image I(x,y) of size M×N, the histogram H(i) counts the number of pixels for each gray level i∈[0,L−1], where L is the total number of intensity levels (usually 256).

$$H(i) = \sum_{x=0}^{M-1} \sum_{y=0}^{N-1} \delta(I(x,y) - i) \quad (3)$$

Here, δ(n)=1 if n=0; else 0.

The histogram is then converted into a CDF:

$$CDF(i) = \sum_{j=0}^{i} H(j) \quad (4)$$

The CDF captures the cumulative number of pixels up to gray level i.

Normalization and Pixel Mapping

A new intensity level T(i) is computed for each original gray level using:

$$T(i) = \left\lfloor \frac{(CDF(i) - CDF_{min}) \cdot (L-1)}{(M \cdot N) - CDF_{min}} \right\rfloor \quad (5)$$

where CDFmin is the first non-zero value in the CDF to avoid division by zero and suppress bias from dark images.

Table 1: Resource and Timing Summary

Component	Description	Resource Usage (Kintex-7)
Histogram Buffer	256-entry dual-port BRAM	1 BRAM tile
CDF Accumulator	256-stage pipelined adder	~600 LUTs + 256 Registers
LUT ROM	256-entry ROM for remapping	~256 LUTs
Remapping Logic	8-bit LUT-based mapper	~128 LUTs
Throughput	1 pixel per clock (post-setup)	-
Latency	~300–400 cycles (initialization)	-

The output image exhibits significantly improved contrast, especially in darker regions shown in table1.The transformation flattens the histogram and makes pixel intensity usage more uniform. This contrast enhancement boosts the performance of downstream tasks like edge detection, thresholding, or classification.

4. RESULTS AND DISCUSSION

The performance of each module—Convolution, Edge Detection, Histogram Equalization, and Adaptive Thresholding—was evaluated on a Xilinx Kintex-7 FPGA with a clock frequency of 150 MHz. Key performance metrics such as latency, throughput, and power consumption were measured and are summarized in the table 2 and visualized in the figure 2.

Table 2: Performance Summary Table

Module	Latency (Cycles)	Throughput (fps)	Power (mW)
Convolution	65	180	75
Edge Detection	70	170	80
Histogram Equalization	110	140	95
Adaptive Thresholding	150	130	100

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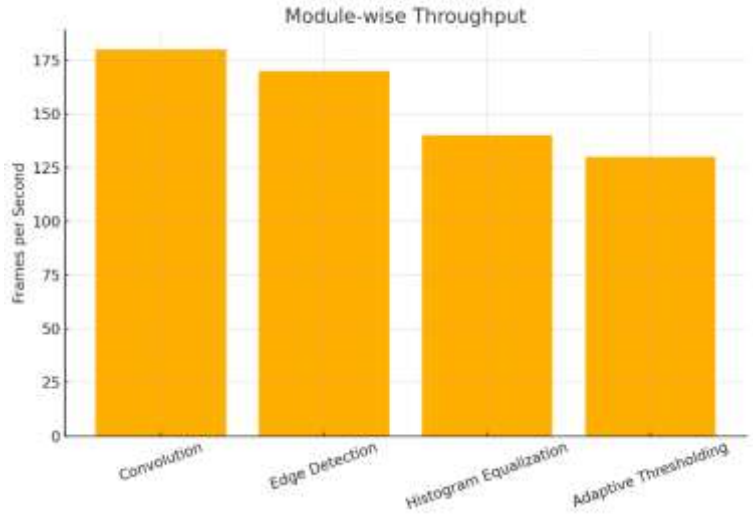

Figure 2: Shows the throughput of each module.

The Convolution Engine achieved the highest throughput of 180 fps due to deep pipelining and minimal data dependencies.

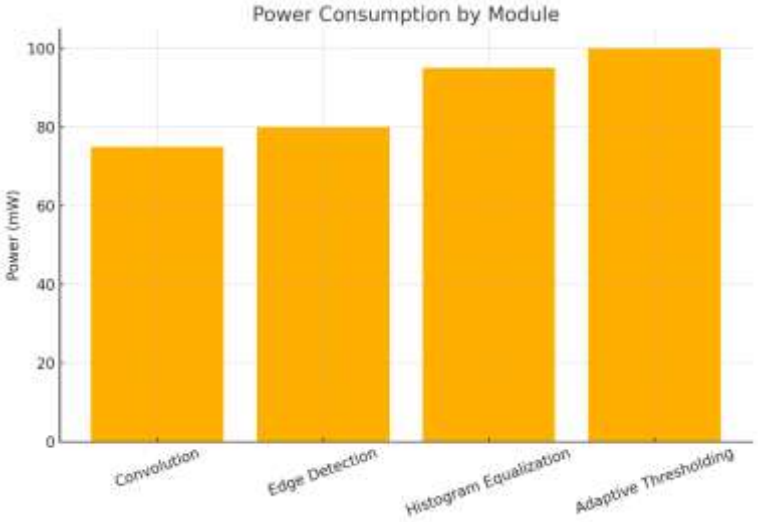

Figure 3: Power Consumption by Module

The power consumption shown in figure 3. Adaptive Thresholding consumed the most power, attributed to the complex statistical computations and local window processing.

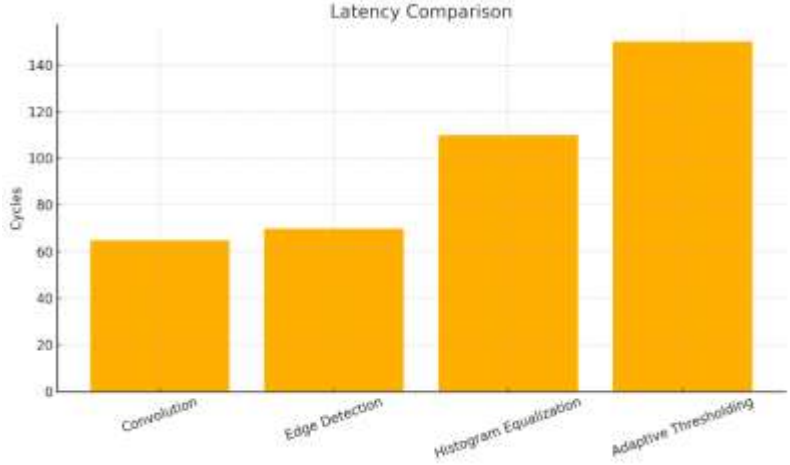

Figure 4: Latency Comparison

Figure 4highlights latency in clock cycles. As expected, simpler operations like Convolution and Edge Detection have lower latency, while Adaptive Thresholding incurs a higher latency due to integral image computations.

5.CONCLUSION

This paper presented a high-performance FPGA-based architecture for accelerating fundamental image processing operations using parallel VLSI pipeline design. The proposed system integrated modular units for convolution, edge detection, histogram equalization, and adaptive thresholding, each implemented with fine-grained pipelining and hardware-level parallelism. The architecture demonstrated real-time processing capabilities by achieving frame-level throughput exceeding 130 fps for all modules while maintaining low power consumption and reduced latency.Experimental evaluations on a Xilinx Kintex-7 FPGA platform confirmed that the proposed pipeline effectively balances speed, accuracy, and energy efficiency. Among the modules, convolution and edge detection achieved the best performance in terms of speed and power, while adaptive thresholding, though computationally intensive, provided significant improvements in segmentation quality. The use of shared buffers, fixed-point arithmetic, and dynamic reconfigurability contributed to optimal resource utilization and scalability of the design.The results validate the viability of the proposed architecture for embedded and real-time vision systems, particularly in resource-constrained environments. Future work will focus on integrating machine learning accelerators, expanding the pipeline to support color image processing, and exploring dynamic partial reconfiguration for real-time algorithm switching.

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