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Design And Evaluation Of Energy-Efficient Approximate Multipliers

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Abstract
Multipliers stand as essential components that play a pivotal role in computational tasks. Their importance is found not just in achieving accurate and high-speed calculations but also in optimizing power efficiency. Approximate multipliers are useful in applications where a modest level of imprecision is tolerated but does not affect the overall outcome. In this paper, two approximate 4:2 compressors are proposed and utilized in an 8×8 Dadda multiplier. By strategically introducing controlled approximations, by sacrificing precision, multipliers with proposed approximate compressors offer reduction in power consumption, area utilization, and delay, by compromising on accuracy. The error analysis is further verified on the scales of Error Rate (ER), Error distance (ED) and multiple other metrics. Xilinx Vivado software is used to simulate and synthesize the proposed designs.

Keywords: *Approximate Multipliers; 4:2 compressors; controlled approximation; Dadda.*

1. INTRODUCTION

Multipliers are key building elements of digital circuits and play a critical role in computational domains. They are utilized across broad spectrum of domains, such as data processing, multimedia technology, signal processing, telecommunications, embedded systems, and VLSI [1]-[8], [13]-[19]. The multiplier precision, speed, and efficiency have a direct impact on the system's overall operation and power consumption [18].

Conventional multipliers place high importance on precision and accuracy, using intricate architectures with error correction and detection mechanisms to guarantee precise outcomes. Conversely, approximate multipliers prioritize efficiency in their design, compromising on accuracy to lower hardware complexity, consume less power, or increase speed. This trade-off makes approximate multipliers to be more useful in situations where a slight accuracy loss is acceptable [10]. For instance, in image processing applications like sharpening, smoothening and transformational operations like filtering, a slight loss in accuracy is tolerable without significantly reducing the image quality [11].

The result from the multipliers is obtained after several stages. These stages include partial products generation, reduction, and accumulation [12], [14], [15]. Usually, the second stage becomes complex. Compressors are the components that count 1's in the inputs and are used in the reduction stage. Approximate compressors provide an innovative approach to reducing the complexity that is typically encountered in the reduction process. Approximate compressors strategically add approximations to the counting of 1's in inputs, resulting in a significant reduction in area, power, and delay, at an acceptable accuracy level.

This paper proposes two of such approximate 4:2 compressors, when implemented in an 8×8 Dadda multiplier, have shown a significant reduction in area, power, and delay, by reducing the accuracy. To determine the error rate and ED from the precise value, the truth tables of the proposed and exact compressors are compared.

This is the arrangement of the remaining paper. Some of the published works on approximation multipliers are reviewed in Section II. The precise compressors and evaluation measures utilised are covered in Section III. The approximate compressors

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proposed are described in Section IV. The analysis and simulation findings are presented in Section V. Finally, Section VI concludes the paper.

2. RELATED WORKS

In recent years, there has been a growing interest in investigating approximate multipliers because of their potential to balance system efficiency requirements with accuracy. Numerous studies were conducted on various aspects of multipliers, optimizing designs and their impact on system performance. Researchers are coming up with different innovative architectures and algorithms to address these challenges. Furthermore, different metrics were used to evaluate the multipliers. Some works that were done are described in this section.

Vigneshwar and Sathish [3] used recursive multiplication by breaking down the inputs into smaller blocks and later adding them. They proposed three new multiplier designs which use approximate 4:2 compressors. Edavoor et al. [7] proposed two new 4:2 approximate compressors and an alternate architecture for multipliers, when three or more compressors are cascaded. Image multiplication was conducted on two images using the suggested approach and compared to alternative designs.Zervakis et al [9] offered a technique that can be used in any architecture. This method skips the generation of partial products therefore decreasing half adders count.

Fang-Yi Gu et al. [17] proposed a technique where partial products can flexibly be truncated based on requirement, also they designed an error compensation circuit to decrease error distance.Gorantla and Deepa [12] implemented their proposed 4:2 approximate compressors and 5:2 approximate compressors in an 8×8 Dadda multiplier.

Pei et al. [2] implemented three approximate 4:2 compressors and presented an error- correcting module in between the approximate compression part and the exact compression part, thereby increasing the accuracy level.

Venkatachalam and Ko [4] proposed a technique where the generated partial products are rearranged according to their weights and XOR gates in adders and compressors which take high area and delay are substituted with AND and OR gates.

3. PRELIMINARIES

3.1. Exact 4:2 Compressor

Compressors compute the sum and carry values at every level, propagating these results to subsequent bits to effectively reduce the partial products formed during multiplication. The exact 4:2 compressor comprises two full adders with five inputs X0, X1, X2, X3 and Cin and three outputs SUM, CARRY, and Cout. Figure 1 represents a block diagram. The outputs come from the below equations:

$$SUM = Cin \oplus X0 \oplus X1 \oplus X2 \oplus X3 \quad (1)$$

$$CARRY = Cin\,(X0 \oplus X1 \oplus X2 \oplus X3) + X3\,(X0 \oplus X1 \oplus X2 \oplus X3) \quad (2)$$

$$Cout = X2\,(X0 \oplus X1) + X0\,(X0 \oplus X1) \quad (3)$$

Compressors are cascaded to one another, and the Cout of the compressor becomes Cin to the next compressor of the next column in the same stage. The SUM is passed on to the same column of the next stage, CARRY is transmitted to the next column of the next stage.

Table 1 is the truth table that depicts its functionality and Figure 2 demonstrates the partial product reduction steps employing exact compressors of an 8×8 Dadda multiplier.

3.2. Evaluation Metrics

To evaluate the effectiveness and quality of the multiplier, various measures are employed. This helps in understanding the effectiveness of the multiplier and gives us a path to compare the exact multiplier with various approximate multiplier. The metrics are :

I. Accuracy metrics: These measures are used to determine the computational accuracy of the multipliers [1],[7]. The metrics for an n-bit multiplier are listed in this paper.

Error Distance (ED): It is the difference between the accurate output and the output that is received from the multiplier. The accurate output is denoted by E_{output} and the obtained value is denoted by O_{output}.

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$$ED = |E_{output} - O_{output}| \quad (4)$$

Table I. Truth Table of Exact 4:2 Compressor

C_{in}	X_0	X_0	X_0	X_0	C_{out}	CARRY	SUM
0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	1
0	0	0	1	0	0	0	1
0	0	0	1	1	0	1	0
0	0	1	0	0	0	0	1
0	0	1	0	1	0	1	0
0	0	1	1	0	1	0	0
0	0	1	1	1	1	0	1
0	1	0	0	0	0	0	1
0	1	0	0	1	0	1	0
0	1	0	1	0	1	0	0
0	1	0	1	1	1	0	1
0	1	1	0	0	1	0	0
0	1	1	0	1	1	0	1
0	1	1	1	0	1	0	1
0	1	1	1	1	1	1	0
1	0	0	0	0	0	0	1
1	0	0	0	1	0	1	0
1	0	0	1	0	0	1	0
1	0	0	1	1	0	1	1
1	0	1	0	0	0	1	0
1	0	1	0	1	0	1	1
1	0	1	1	0	1	0	1
1	0	1	1	1	1	1	0
1	1	0	0	0	0	1	0
1	1	0	0	1	0	1	1
1	1	0	1	0	1	0	1
1	1	0	1	1	1	1	0
1	1	1	0	0	1	0	1
1	1	1	0	1	1	1	0
1	1	1	1	0	1	1	0
1	1	1	1	1	1	1	1

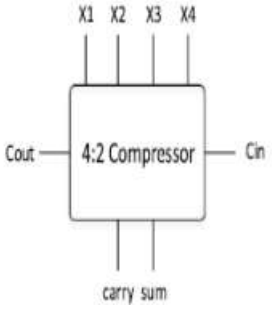

Fig. 1. Exact 4:2 Compressor Block Diagram[20]

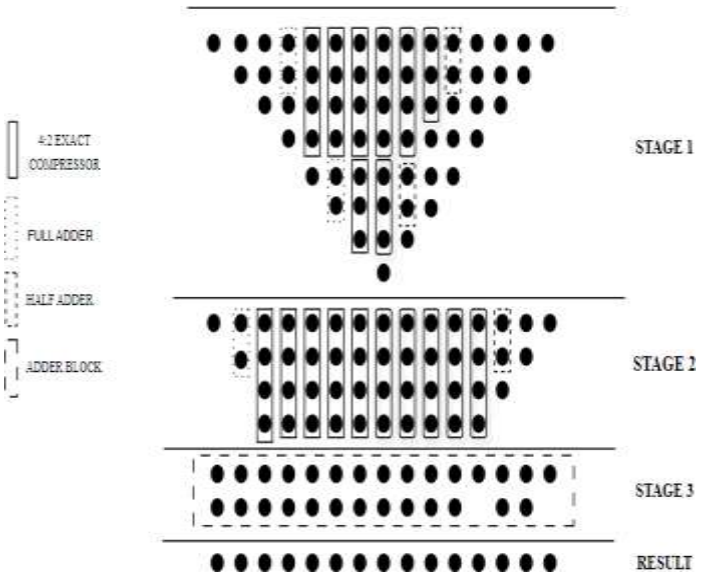

Fig. 2. Dadda multiplier using Exact 4:2 Compressors

Mean Error Distance (MED): MED quantifies the average distance between the exact value and the obtained value. It is calculated by summing the differences and then dividing by the total possible cases. A lower value of MED indicates a higher level of accuracy. EDj represents the error distance between the jth accurate and obtained value.

$$MED = \frac{1}{2^{2n}} \sum_{j=1}^{2^{2n}} |ED_j| \quad (5)$$

Mean relative error distance (MRED): The absolute relative error is obtained by dividing the absolute difference between the obtained and exact values by the exact value. The mean of these values gives MRED. A lower MRED signifies a higher level of accuracy.

$$MRED = \frac{1}{2^{2n}} \sum_{j=1}^{2^{2n}} \frac{ED_j}{E_{output\,j}} \quad (6)$$

Normalised mean error distance (NMED): This is obtained by averaging the values obtained by dividing the error by the maximum possible error. A lower value of NMED indicates higher accuracy.

$$NRED = \frac{1}{(2^n+1)^2} \frac{\sum_{j=1}^{2^{2n}} ED_j}{2^{2n}} \quad (7)$$

Accurate output count (AOC): AOC represents the output values that are accurate from the total possible cases. A higher AOC indicates a higher level of accuracy, signifying that the approximate multiplier produces a significant proportion of correct results despite its approximations.

II. **Implementation metrics:** These metrics give an understanding of the resource utilization. This includes power, area, and delay.

a) **Power:** When evaluating the multiplier design, power consumption is a crucial factor. It includes total power consumption, static power, and dynamic power. Dynamic power is the power consumed due to logic operations, input/output activities, and signal switching. The dynamic power consumption varies according to the frequency of operations and the computational workload. The power used even when the multiplier is not actively processing data is known as static power. Leakage currents and other non-switching power factors are taken into consideration. Dynamic and static powers, when combined, give total power.

b) **Area:** The representation of area utilization is expressed in the number of Look-Up Tables (LUT). LUTs are fundamental building blocks in FPGA technology, used to implement logic functions and store data. Each LUT has a specific size and can be configured to perform various logic operations based on its inputs. The relationship between area and LUTs in FPGA design is intertwined, as a higher number of LUTs generally corresponds to

increased area utilization.

c) **Delay:** The time taken by the multiplier to produce the output after receiving the input values is given by delay. The multiplier's processing speed for inputs and outputs is directly affected by the delay. The logic delay describes the amount of time taken by signals to pass through the multiplier's logic gates. The time taken by signals to move between various multiplier components via routing pathways, like wires and interconnects, is known as the route delay. The total delay refers to the total of both delays.

4. PROPOSED APPROXIMATE COMPRESSORS

The process of approximation involves eliminating the Cout output of the compressor, thereby decreasing the total number of outputs produced by the compressor [6],[7]. An error occurs solely when all the input bits are 1's that is, when the input is 1111, resulting in an ED of -1. Two designs of approximate 4:2 compressors are proposed in this paper, Table 2 is the truth table of the proposed compressors. The inputs of the proposed approximate 4:2 compressors are X0, X1, X2, X3 and the outputs are SUM (S) and CARRY (C).

A. Proposed Design 1 (D1)

The gates in D1 is less than the number of gates in the exact compressor. Figure 3 gives the logical representation of D1. The equations for outputs are

$$S = X0\ X1 + X2\ X3 + ((X0 + X1) \oplus (X2 + X3)) \quad (8)$$

$$C = X0\ X1 + X2\ X3 + (X0 + X1)(X2 + X3) \quad (9)$$

Errors are produced when the inputs of the compressor are {0011}, {1100}, {1111} with an ED of (1, 1, -1) respectively. The proposed design D1 has an error rate of 18.75%.

B. Proposed Design 2 (D2)

The output carry of D2 is simply replaced with an OR gate between X2 and X3, hence reducing the gates. It's logical representation is given by Figure 4.

$$S = (X2 \oplus X3)(X0 + X1) + X0\ X1 \quad (10)$$

$$C = X2 + X3 \quad (11)$$

Errors are produced when the inputs are – {0001},{0010}, {1100}, {1111} with an ED of (1, 1, -1, -1) respectively. This design has an error rate of 25% is greater than D1, which suggests that accuracy of D1 is greater than D2

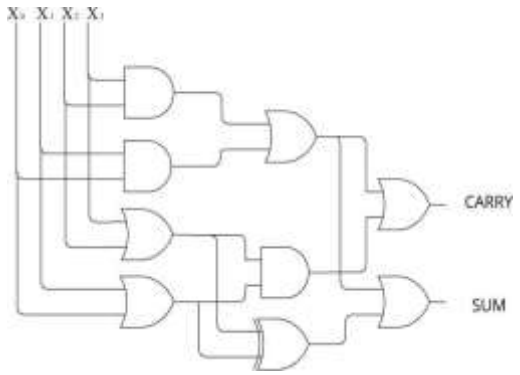

Fig. 3. Proposed approximate 4:2 compressor (D1)

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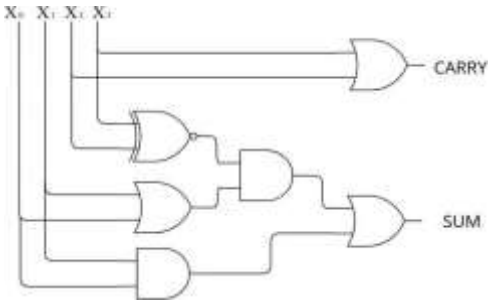

Fig. 4. Proposed approximate 4:2 compressor (D2)

TABLE II. TRUTH TABLE OF PROPOSED 4:2 COMPRESSORS

				D1			D2		
X0	X1	X2	X3	C	S	ED	C	S	ED
0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	1	0	1
0	0	1	0	0	1	0	1	0	1
0	0	1	1	1	1	1	1	0	0
0	1	0	0	0	1	0	0	1	0
0	1	0	1	1	0	0	1	0	0
0	1	1	0	1	0	0	1	0	0
0	1	1	1	1	1	0	1	1	0
1	0	0	0	0	1	0	0	1	0
1	0	0	1	1	0	0	1	0	0
1	0	1	0	1	0	0	1	0	0
1	0	1	1	1	1	0	1	1	0
1	1	0	0	1	1	1	0	1	-1
1	1	0	1	1	1	0	1	1	0
1	1	1	0	1	1	0	1	1	0
1	1	1	1	1	1	-1	1	1	-1

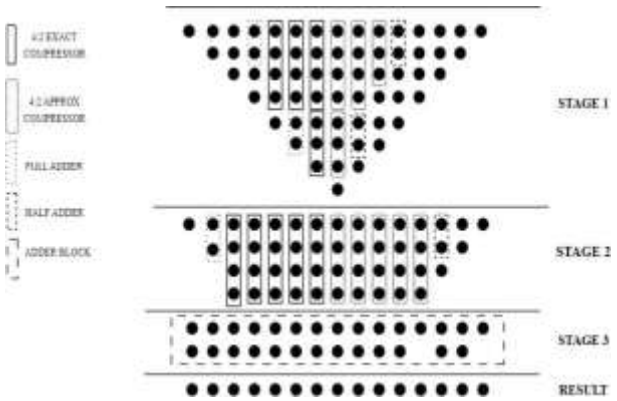

Fig. 5. Dadda multiplier using exact and proposed approximate compressors (exact towards left and approximate towards right)

Figure 5 shows how the designs are integrated into Dadda multiplier. Since the least order bits contribute less value to the result, the proposed designs are employed in the first half columns of the multiplier and exact compressors are integrated in the remaining higher order bit columns, emphasizing precision and accuracy in the result. This strategic allocation optimizes the implementation and accuracy efficiency.

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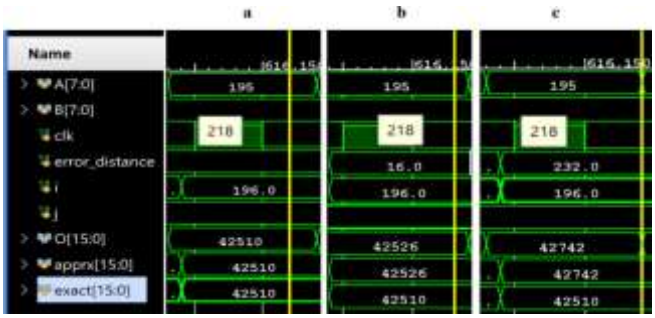

Fig. 6. Simulation result by multiplying two 8 bit numbers A and B, using Dadda multiplier with different compressor designs (a) exact compressor (b) D1 (c) D2

5. RESULTS

This section presents the simulation results and analysis of obtained results by implementing the proposed 4:2 compressors in 8×8 Dadda multiplier. The efficiency of the multiplier is analysed under different implementation metrics, and finally checking the accuracy effectiveness of the multiplier using accuracy metrics. All the simulations are carried out in Xilinx Vivado for Artix 7 board family, with default parameter settings.

A. Simulation results:

All the multipliers, exact 8×8 Dadda multiplier and approximate multipliers implemented using D1 and D2 each, are simulated. The generated waveforms during simulation represent the Ooutput of the above multipliers, as in Figure 6.

B. Implementation Analysis of 8×8 Dadda multiplier using exact and proposed compressors

After synthesis of the designs, this implementation analysis aims to analyse the performance of the multipliers, using the obtained results.

Power: The power consumed by Exact Multiplier and proposed designs shown in figures 7- 9 and are listed in the Table 3 . The total power consumed by the multiplier with proposed compressors is significantly less than the design with the exact compressor. The power consumed by D2 is even less than that of D1, showing that D2 is more power efficient than D1.

Fig 7. Power consumed by Exact multiplier

Fig 8. Power consumed by Multiplier with proposed design 1

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Fig 9. Power consumed by Multiplier with proposed design 1

TABLE III. POWER CONSUMED

Compressor design used	Dynamic Power			Static Power (W)	Total Power (W)
	Signals (W)	Logic (W)	I/O (W)		
Exact	0.849	0.754	12.670	0.219	14.493
D1	0.671	0.503	12.458	0.203	13.836
D2	0.556	0.450	11.857	0.185	13.048

Area: The number of LUTs utilized by Exact Multiplier and proposed multiplier designs shown in figures 10-12 and are listed in Table 4. Number of LUTs occupied by multiplier with exact compressor design is higher than multiplier with proposed compressor designs. Mainly, the LUTs with 6 and 5 inputs which occupy more area are noticeably higher for exact design. The LUTs utilized by the D1 is more than D2, showing that D1 is more resource- efficient than D1, and both are more resource- efficient than the exact design

Ref Name	Used	Functional Category
LUT6	46	LUT
LUT5	22	LUT
LUT4	18	LUT
OBUF	16	IO
IBUF	16	IO
LUT2	14	LUT
CARRY4	4	CarryLogic
LUT3	1	LUT

Fig 10. LUTs occupied by Exact Multiplier

Ref Name	Used	Functional Category
LUT6	36	LUT
LUT2	21	LUT
OBUF	16	IO
IBUF	16	IO
LUT5	15	LUT
LUT4	9	LUT
CARRY4	4	CarryLogic
LUT3	1	LUT

Fig 11. LUTs occupied by Multiplier with proposed design 1

Ref Name	Used	Functional Category
LUT6	26	LUT
LUT5	19	LUT
OBUF	16	IO
IBUF	16	IO
LUT4	15	LUT
LUT2	9	LUT
CARRY4	4	CarryLogic
LUT3	1	LUT

Fig 12. LUTs occupied by Multiplier with proposed design 2

TABLE IV. LUTS UTILIZED

Compressor design used	Type of LUT used					Total LUTs as Logic
	LUT6	LUT5	LUT4	LUT3	LUT2	
Exact	46	22	18	1	14	101
D1	36	15	9	1	21	82
D2	26	19	15	1	9	70

Delay: The delay caused due to logic, routing and the total delay for Exact Multiplier and proposed multiplier designs shown in figures 13-15 and are tabulated in Table 5. The delay that occurred in the exact compressor design is higher than proposed D1 and D2, which suggests the proposed designs have faster signal propagation and computation times.

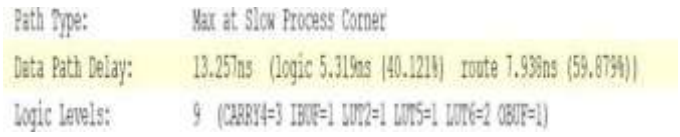

Fig 13. Delay caused in Exact Multiplier

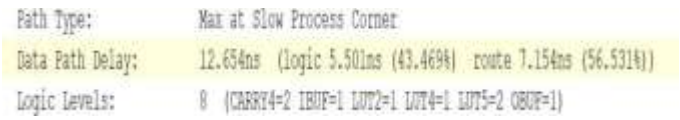

Fig 14. Delay caused in Multiplier with Proposed Design 1

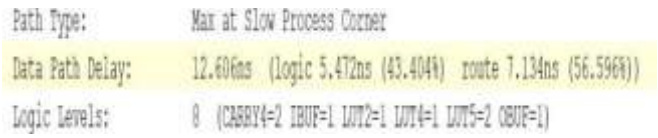

Fig 15. Delay caused in Multiplier with Proposed Design 2

TABLE V. DELAY CAUSED

Compressor design used	Delay		Total Delay (ns)
	Logic (ns)	Route (ns)	
Exact	5.319	7.938	13.257
D1	5.501	7.153	12.654
D2	5.472	7.134	12.606

A. Accuracy analysis of 8×8 Daddamultiplier using exact and proposed compressors

The accuracy analysis is done to ensure the precision and correctness of the proposed design. This analysis gives an idea how near the multiplier using designed compressor can produce the output to that of the exact design. Table 6 lists all the accuracy metrics and their values for all the designs.

The MRED and NMED are notably lower for D1 than D2, signifying a closer match between the exact output and the obtained result. Furthermore, the AOC of D1 is high, which signifies D1 produces more number of accurate results.

TABLE VI. ACCURACY METRICS

Compressor design	MED	MRED	NMED	AOC

used				
D1	46.2712	0.0095	0.0007	34948
D2	113.9063	0.0376	0.0017	8363
Edavoor[7] et.al	573.4	0.0487	-	7782

6. CONCLUSION

The paper presents two 4:2 approximate compressor designs both aimed on reducing the resource requirements maintaining acceptable level of accuracy. Firstly, the design D1 with an Error Rate of 18.75%, produced least values of MRED, MED and NMED which suggests that the proposed design have a high accuracy, closely approximating the results to the exact design. In contrast, the second design produces comparably low accuracy than D1, but is more efficient in terms of power, area and delay, indicating its priority towards resource optimization. Overall, Design D1 is appropriate for applications where precision is critical because it places a high priority on accuracy and maintains a high degree of fidelity to the exact design. However, the second design caters to scenarios where resource constraints and performance optimizations take precedence, sacrificing some accuracy in favor of increased efficiency.

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