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Analysis And Optimization Of Two-Stage OTA Architectures For Power-Efficient Amplification

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Abstract
This work presents the design, simulation, and performance evaluation of two-stage Operational Transconductance Amplifiers (OTAs)—specifically a single-ended and a fully differential configuration—implemented in 45nm CMOS technology for low-power applications. Emphasizing biomedical and IoT-integrated systems, the study adopts a simulation-driven methodology using Cadence Virtuoso and Spectre. Key performance parameters such as gain, bandwidth, common-mode rejection ratio (CMRR), power consumption, and offset voltage were analyzed and compared. The fully differential OTA achieved superior noise immunity and energy efficiency with a CMRR of 100 dB and power consumption of just 28 µW, while the single-ended OTA offered a slightly higher gain of 57 dB. These findings validate the suitability of the proposed designs for energy-constrained, high-precision analog front-end applications.
Keywords: *Operational Transconductance Amplifier, CMOS, Low Power, Biomedical Electronics, Differential Amplifier, Cadence, Spectre, CMRR, OTA Design.*

INTRODUCTION

With the rapid scaling of CMOS technology, the design of analog circuits in lower technology nodes (sub-45 nm and beyond) has become both an opportunity and a challenge in modern integrated circuit (IC) design. Lower technology nodes enable higher transistor density, faster switching speeds, and reduced dynamic power consumption, which are advantageous for digital circuits. However, analog circuit design faces significant difficulties due to reduced intrinsic gain, lower output resistance, increased device mismatches, higher leakage currents, and lower supply voltage headroom. As supply voltages decrease while threshold voltages remain relatively constant, designing analog blocks such as operational trans conductance amplifiers (OTAs), comparators, and filters becomes more complex. The reduced voltage headroom constrains signal swing, while short-channel effects degrade performance parameters like gain and noise. Despite these challenges, the demand for low-power, high-performance analog systems in applications such as IOT, biomedical sensing, and wireless communication has driven the need for innovative analog design techniques tailored for advanced CMOS nodes.

This work focuses on exploring methodologies and circuit topologies optimized for lower technology nodes, aiming to overcome performance degradation and leverage scaling advantages. Emphasis is placed on key analog performance metrics such as gain, bandwidth, linearity, noise, power efficiency, and layout considerations, all within the constraints posed by modern CMOS technologies.

Analog VLSI and OTA Design Basics:

Analog VLSI design remains foundational to real-world signal processing, interfacing between physical signals and digital computation. Within this domain, Operational Transconductance Amplifiers (OTAs) are vital building blocks used for amplification, filtering, and signal transformation (Li et al., 2021) . OTAs differ from conventional op-amps as they act as voltage-controlled current sources, suitable for high-frequency and low-power applications. Differential amplifiers are another key circuit that improves noise immunity and allows balanced signal processing. The transition to advanced nodes such as 45nm CMOS intensifies challenges in analog design due to reduced gain, higher leakage, and voltage constraints.

Low-Bandwidth Applications:OTAs and differential amplifiers find crucial roles in low-bandwidth analog domains such as biomedical electronics, where signals such as ECG, EEG, and EMG need accurate, low-noise amplification. These circuits must operate with high precision at low frequencies and under stringent power budgets, often powered by batteries or energy-harvesting units. Differential architectures help suppress common-mode noise, making them well-suited for such sensitive tasks.

Power-Aware OTA and Differential Designs:

In modern analog ICs, power-aware design strategies are critical. This includes optimizing transistor sizing, biasing currents, and layout to achieve minimal static and dynamic power dissipation. OTAs must achieve an optimal balance between gain, bandwidth, and power consumption (Tripathy et al., 2021). Two-stage architectures, especially in 45nm technology, allow the cascading of gain stages to achieve high amplification without sacrificing power efficiency.

Proposed Method for Biomedical Applications:

The proposed OTA architectures are tailored for biomedical systems that require high gain, low noise, and minimal power. In such environments, fully differential OTAs improve signal quality by eliminating common-mode interference, while maintaining low offset voltages—essential for accurate signal reproduction.

OTA in Wearable and Implantable Devices:

In wearable biosensors and implantable devices, battery life and thermal dissipation constraints necessitate circuits like fully differential OTAs that consume minimal power without compromising performance. This paper demonstrates designs that can meet these demands within the 45nm node, showing their suitability for such applications.

Role in IoT-Integrated Health Monitoring:

With the rise of IoT-integrated medical diagnostics, the need for robust analog front-end circuitry is growing. Our proposed OTAs, optimized in 45nm CMOS, serve as potential solutions for edge-level data processing in smart healthcare monitoring systems, enabling continuous real-time biosignal acquisition with high fidelity(Kumari et al., 2021).

RELATED WORK

Operational Transconductance Amplifiers (OTAs) are crucial components in analog Very Large Scale Integration (VLSI) design, acting as voltage-controlled current sources. Research papers in this field often focus on novel design methodologies, performance optimization (e.g., low power, high linearity, wide bandwidth), and various applications within analog and mixed-signal circuits. The aim is to create OTAs that meet the evolving demands of modern VLSI technology, such as reduced size, lower power consumption, and improved performance metrics. Operational Transconductance Amplifier (OTA) is one of the most versatile and important circuit components in the analog and mixed signal circuit design. It is also one of the more complex cells to design. Basically there are many types of op-amp but OTA is different from others because OTA is voltage control current source device. For OTA, input will be voltage at different types and achieved current at output side (Goswami et al., 2021). The main feature of paper is that it reduces the size of chip decreasing MOS transistor in conventional design of OTA which have 16 and our design reduce MOS transistor up to 10 and it reduce noise up to some extent and try to get good design which has higher output capability. This paper gives analysis of Schematic design and CMOS Layout of OTA for different types of inputs and gets parameter like Gain margin, Phase margin, Slew Rate, CMRR, Transient Time, Noise Spectral Density, PSRR, Power Dissipation and Power Consumption. The operational transconductance amplifier (OTA) is one of the most important basic blocks used in the design of analog integrated circuits (ICs). However, its optimization involves a large number of parameters and specifications that have to be accurately adjusted during the simulation process to appropriately achieve the design goals. This work addresses the whole framework required to the automatic design of an OTA, from its architecture to manufacturing. In this Paper we represent designing of different types of OTA amplifier along with their advantages and disadvantages by use of various techniques (Xu et al., 2021).

OTA-Based Research:
Operational Transconductance Amplifiers have been a key topic in analog VLSI literature, with research exploring low-voltage, low-power, and high-linearity design strategies. Notable works include OTA designs optimized for rail-to-rail input, low distortion, and biasing techniques that improve gain while conserving power. Techniques such as dynamic biasing and gain-boosting are widely explored.

Single-Ended OTA Studies:
Several designs using single-ended OTAs focus on layout simplicity, small chip area, and integration in low-cost applications. Despite their reduced noise immunity compared to differential designs, single-ended OTAs offer adequate performance for many sensor and control applications, especially where signal environments are relatively clean.

Fully Differential Amplifier Studies:
Fully differential OTAs are favored in precision analog systems due to their superior CMRR and PSRR. Literature includes designs employing common-mode feedback, symmetric layout strategies, and adaptive biasing for improved performance under process-voltage-temperature (PVT) variations (Das et al., 2021). These architectures are well-suited for instrumentation-grade amplifiers.

Power-Efficient, Application-Oriented Designs:
Recent research emphasizes energy-aware amplifier design for portable electronics. Innovations include nano-power OTAs for wearable EEG/ECG circuits and ultra-low-leakage biasing methods. These works align with the goals of our paper—delivering compact, high-gain circuits with minimal power draw, validated under biomedical use cases.

DESIGN METHODOLOGY

The present study adopts a simulation-driven, performance-optimized design methodology to develop two types of two-stage Operational Transconductance Amplifier (OTA) architectures**: a single-ended output OTA** and a **fully differential output OTA**, both implemented in **45nm CMOS technology** (Pavithra et al., 2021). The design process was carried out using industry-standard tools—**Cadence Virtuoso** for schematic design and layout, and **Spectre simulator** for circuit analysis and performance evaluation. This combination allows accurate modeling of deep-submicron effects, device non-idealities, and parasitic interactions that critically influence analog circuit behavior in advanced nodes. The design process began with the development of circuit schematics for both the single-ended and fully differential OTA topologies. In the single-ended design, a classic two-stage architecture was employed: the first stage comprises a differential input pair with active load, while the second stage is a common-source amplifier that boosts the gain. For the fully differential OTA, a symmetric dual-output structure was adopted with common-mode feedback (CMFB) circuitry to stabilize the output common-mode level. Both topologies were designed with low-voltage operation in mind, given the reduced headroom constraints of 45nm technology, where supply voltages are typically limited to around 1.3V. Careful **transistor sizing and W/L (width/length) ratio selection** played a central role in meeting performance targets (Kumar et al., 2021). The sizing process aimed to strike a balance between transconductance, output resistance, speed, and power consumption. Larger channel widths were assigned to input pair transistors to maximize transconductance and reduce input-referred noise, while minimum channel lengths (200nm) were used to preserve high-speed operation. In current mirror and load stages, the sizing was optimized to reduce mismatch and ensure current stability. The **biasing strategy** was based on constant current biasing through current mirrors and tail current sources. In the fully differential OTA, additional biasing considerations were required to power the CMFB loop without compromising dynamic range. The bias circuits were designed to consume minimal power while maintaining operational stability across process-voltage-temperature (PVT) variations. A current of 10 μA was maintained as the design reference to limit power dissipation, and all circuits operated at a nominal supply voltage of 1.3V. Following schematic-level validation, **DC, AC, transient, noise, and parametric simulations** were performed using the Spectre simulator. The **DC analysis** validated bias points, voltage levels, and power dissipation (Tripathi et al., 2021). **AC analysis** provided key frequency-domain parameters such as open-loop gain, phase margin,

bandwidth, and unity gain frequency. **Transient simulations** tested time-domain response, slew rate, and settling time. Additionally, **noise simulations** were run to estimate input-referred noise and noise spectral density, which are critical for analog front-end circuits in biomedical and sensor applications.
The methodology thus combines theoretical circuit analysis, simulation-based optimization, and layout-driven validation to deliver OTA designs that are not only power-efficient but also robust under advanced CMOS constraints. The final designs serve as viable analog building blocks for integration in low-power biomedical and IoT-oriented system-on-chip platforms.

1. Two stage single ended OTA :

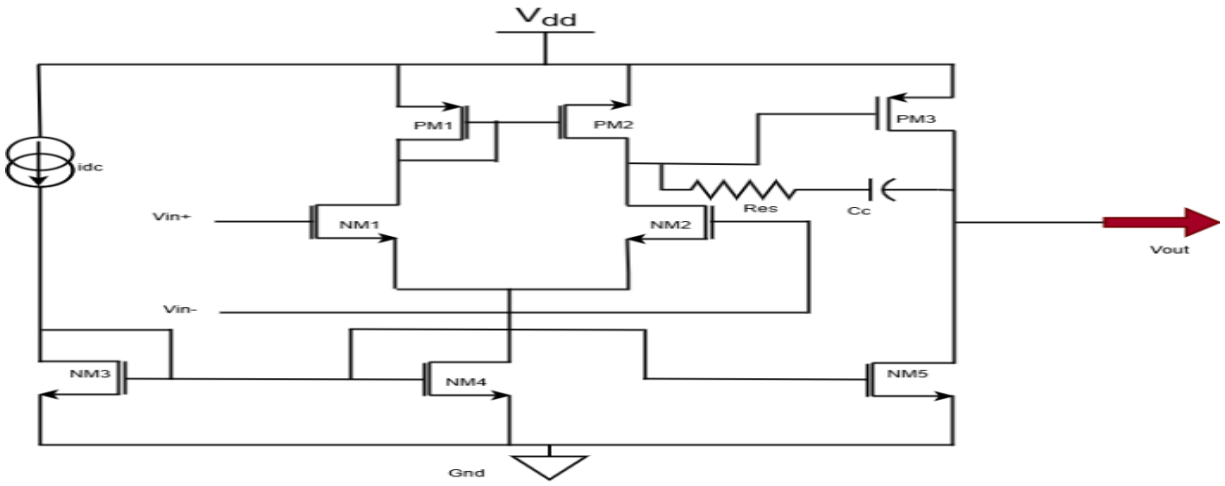


Fig.1: Two stage single ended OTA circuit diagram

The single-ended OTA consists of two main stages:

1. First Stage:
The initial amplification is performed by a differential input stage composed of NMOS transistors (NM0 and NM1), paired with PMOS current mirror loads (PM0 and PM1). This configuration effectively processes and amplifies the differential input signal.
2. Second Stage:
The output gain is further increased by a common-source amplifier stage, typically implemented with transistor NM3. The biasing circuitry, which includes PM2 along with NM4 and NM5, ensures stable operating currents and enhances overall stage performance.
This two-stage architecture is optimized to achieve high voltage gain, while maintaining a balance between bandwidth and power efficiency, especially in systems constrained by a low supply voltage of 1.3V.
Formulas of Two stage Single Ended OTA's:

1. Output Voltage:
Assuming a small signal Differential input $V_{in} = V_{in+} - V_{In-}$
And the output voltage is $V_{out} = A_V . V_{in}$

2. Gain:
The overall gain A_V is the Product of the gain of both stages $A_V = A_{V1} . A_{V2}$
A_{V1}: First Stage gain (Differential pair with Load)
A_{V2}: Second Stage gain (Common Source Stage)

$$A_{V1} = g_{m1} . R_{out1}$$

g_{m1}: Input differential pair of transconductance
R_{out1}: Output Resistance of the first stage

$$R_{out1} \approx r_{ON} || r_{OP}$$

$$A_{V2} = g_{m2} \cdot R_{out2}$$

g_{m2}: Transconductance of second stage
R_{out2}: Output Resistance of the second Stage

$$R_{out2} \approx r_O || R_L$$

Total Voltage Gain $(A_V) = (g_{m1} \cdot R_{out1}).(g_{m2} \cdot R_{out2})$

3. Phase Margin:

Phase Margin determines the stability of the amplifier.

$$PM \approx 90^0 - \tan^{-1}(\frac{g_{m2}}{2\pi f_u C_L})$$

Or, using dominant pole approximation and second pole fp:

$$PM \approx 90^0 - \tan^{-1}(\frac{f_p}{f_u})$$

f_p: Second pole(often due to the output node capacitance)
f_u: Unity gain frequency

4. Bandwidth:

In a Two stage OTA , the frequency response is dominated by two poles due to its cascaded structure.

First [Dominant] pole: $f_{p1} = \frac{1}{2\pi R_1 C_{eq}} = \frac{1}{2\pi R_1 C_C (1+A_{v2})}$

R_1: Output Resistance of First stage
Cc: Compensation Capacitor
A_{v2}: Second stage Gain

Second [Non-Dominant] pole: $f_{p2} \approx \frac{1}{2\pi R_2 C_L}$

R_2: Output resistance of second stage
C_L: Load capacitance [External +parasitic]

5. Unity Gain Frequency:

The UGF (also called gain-bandwidth product) is the frequency at which the gain of the OTA drops to 1 (0 dB).

$$f_u = \frac{g_{m1}}{2\pi C_C}$$

- g_{m1}: Transconductance of the input differential pair
- C_C: Compensation capacitor (Miller capacitor)

6. Common Mode Rejection Ratio (CMRR):

CMRR (dB) = $20\log_{10}(\frac{A_d}{A_{cm}})$

Differential Gain $(A_d) = g_{m1} R_{out1} . g_{m2} R_{out2}$ [product of both stages]

Common Mode Gain $(A_{cm}) \approx \frac{1}{2} \frac{g_{m1} r_{o1}}{1+2g_m r_{tail}} (\frac{r_{o2}}{r_{o2} || R_L})$

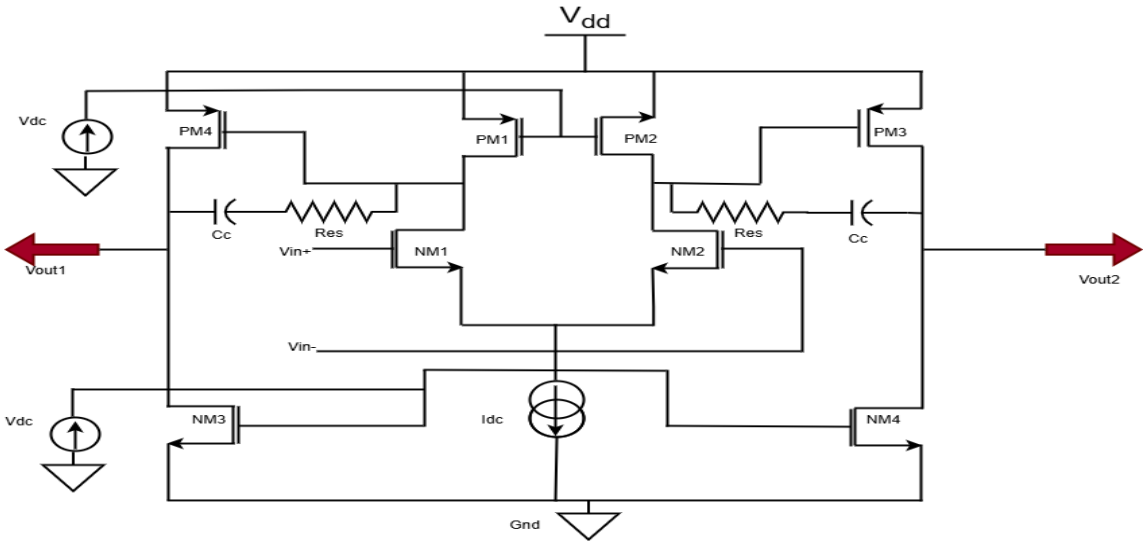
The Dominant term is set by the finite output resistance of the tail current source and of the second stage bias device.

CMRR$\approx 2g_{m1} r_{tail}$

7. Offset Voltage:

$$V_{OS} = \text{common mode input voltage} / 20\log_{10}(\frac{A_d}{A_{cm}})$$

8. Output Power:



$$P_{total} = V_{DD}(I_{bais1} + I_{bias2})$$

V_{DD}: Supply voltage of two stage single ended OTA
I_{bais1} and I_{bias2}: Bias Currents of first stage and second stage

2. Two stage Fully Differential OTA:

Fig.2: Two stage Fully Differential OTA circuit diagram

Fully Differential Two-Stage OTA:

The fully differential OTA is an extended version of the single-ended design, incorporating key enhancements for improved performance:

1. **Balanced Dual Outputs:** It features two symmetrical output branches formed by an NMOS differential input pair (NM0, NM1) and matched PMOS active loads (PM0, PM1), ensuring equal and opposite signal paths for high accuracy.
2. **Common-Mode Feedback (CMFB)**: A dedicated feedback mechanism is employed to regulate the common-mode voltage, thereby preserving output symmetry and consistent voltage swing.
3. **Differential Second Stage:** Transistors NM3 and NM4 serve as the second amplification stage, providing additional gain while maintaining differential signal characteristics.

This architecture improves linear response, enhances the Common-Mode Rejection Ratio (CMRR), and ensures high signal integrity, which is particularly valuable in low-noise applications such as biomedical instrumentation.

Formulas of Two stage Fully differential OTA here it is

1. Output voltage :

In a fully differential OTA, the output is the difference between the voltages at the two output nodes:

$$V_{Out} = V_{out2} - V_{out1}$$

$V_{out2} - V_{out1}$: Voltages at the two symmetric output branches

2. Gain:

$A_V = (g_{m1} \cdot R_{out1}) \cdot (g_{m2} \cdot R_{out2})$

g_{m1}: Transconductance of the input differential pair
g_{m2}: Transconductance of the second stage

R_{out1} and R_{out2}: Output resistances of each stage

3. **Phase Margin:**

$$PM \approx \tan^{-1}\left(\frac{f_p}{f_u}\right)$$

4. **Bandwidth:**

$f_{3dB} \approx \frac{1}{2\pi R_2 C_L}$ or $f_{3db} \approx \frac{g_{m1}}{2\pi C_C}$

5. **Unity gain frequency:**

$$f_u = \frac{g_{m1}}{2\pi C_C}$$

6. **CMRR:**

CMRR (dB) = $20\log_{10}\left(\frac{A_d}{A_{cm}}\right)$

7. **Offset Voltage:**

$$V_{OS} = \text{common mode input voltage} / 20\log_{10}\left(\frac{A_d}{A_{cm}}\right)$$

8. **Power:**

$$P_{Total} = V_{DD}(I_{total})$$

V_{DD}: supply voltage of Two stage Fully Differential OTA
I_{total}: Total current drawn (from both stages + bias circuitry)

RESULT AND DISSCUTIONS

1. **Two stage single ended OTA:**

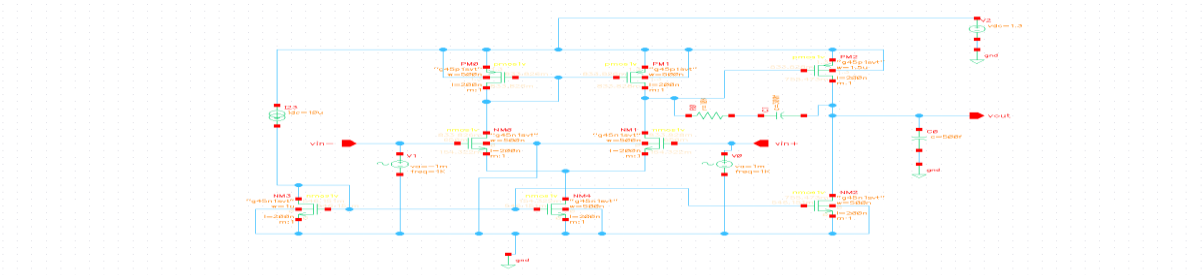


Fig.1: Two stage single Ended OTA

This schematic illustrates a two-stage single-ended Operational Transconductance Amplifier (OTA). The first stage is a differential pair (NM0, NM1) with an active PMOS current mirror load (PM0, PM1). The second stage is a common-source amplifier (NM2) with an active PMOS load (PM2). Miller compensation (C1, R0) is implemented between the stages for stability, and the circuit uses current sources (ID0) and diode-connected transistors (NM3, NM4) for proper biasing, delivering a single-ended output at Vout.

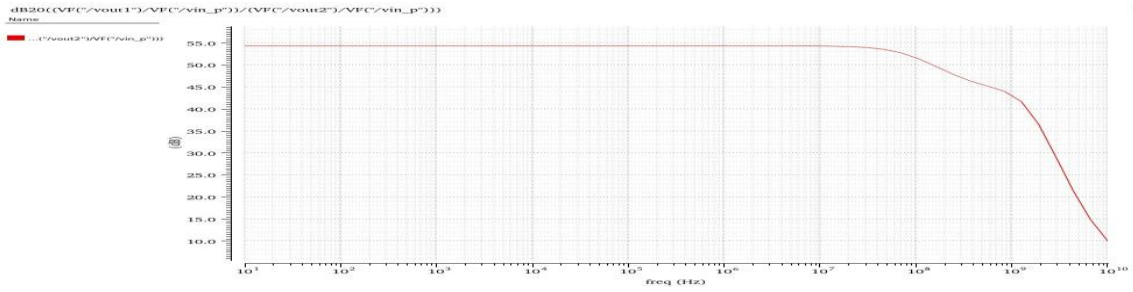
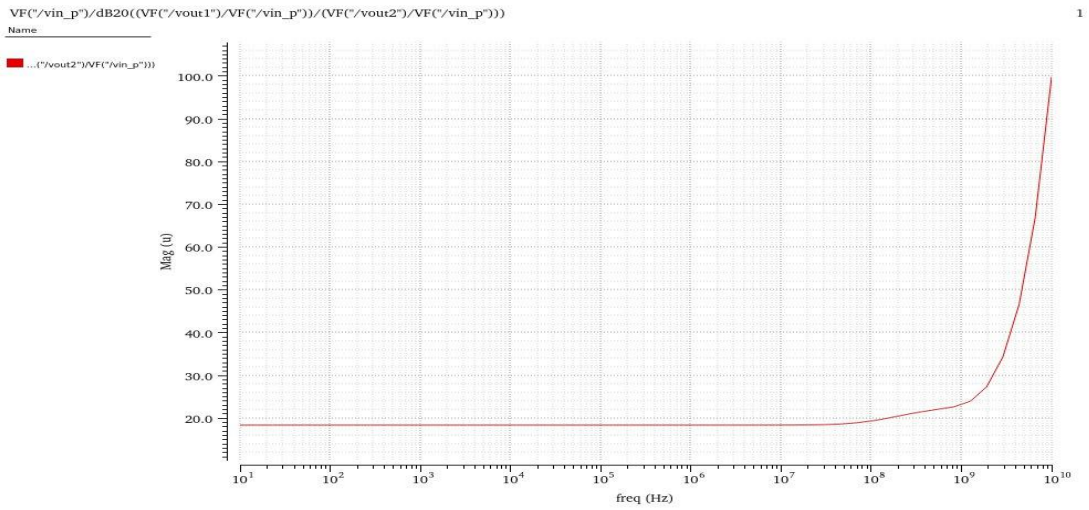


Fig 2: Two stage single ended OTA CMRR waveform

This graph



represents the frequency response (gain vs. frequency) of an OTA (Operational Transconductance Amplifier), likely in a fully differential configuration. The gain remains flat at approximately 55 dB across low and mid frequencies, indicating stable amplification. A noticeable roll-off begins near 10^7 Hz (10 MHz), defining the bandwidth of the amplifier. Beyond this, the gain drops sharply, reflecting the amplifier's cutoff frequency and high-frequency limitations.

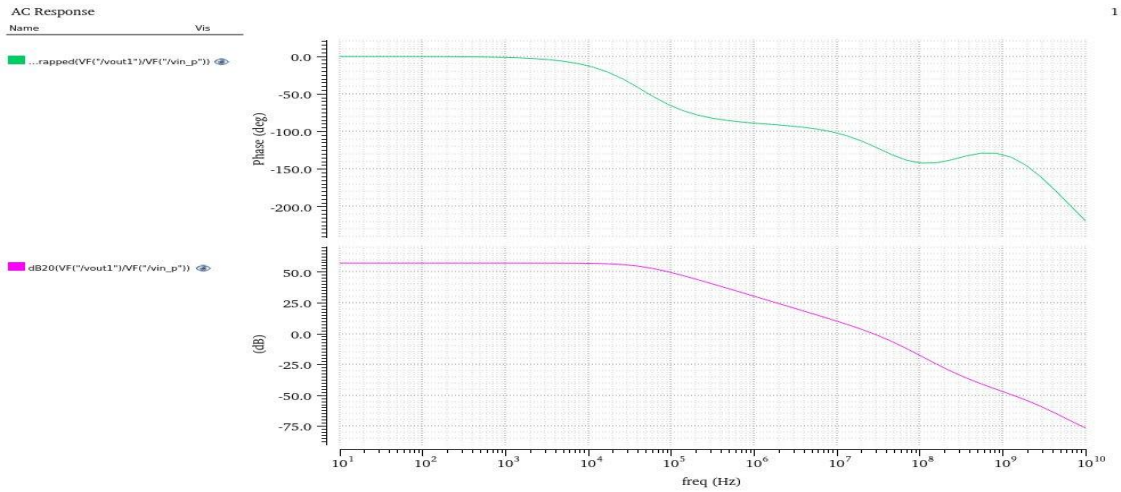


Fig3: Two stage single ended OTA Gain and Phase margin

This AC response graph illustrates both the gain (bottom plot) and phase (top plot) of the OTA across frequency. The gain remains steady around 55 dB at low frequencies and starts rolling off beyond ~10^5 Hz, indicating the bandwidth limit. The phase shift becomes more negative with increasing frequency, reflecting the amplifier's frequency-dependent delay. The curve indicates a typical two-stage OTA behavior, with dominant and non-dominant

Fig4: Two stage single ended OTA offset voltage

The graph displays the frequency-dependent magnitude response of the offset voltage in a two-stage single-ended OTA. The vertical axis shows the magnitude in decibels (dB), while the horizontal axis spans frequencies from 10 Hz to 10 GHz. At lower and mid frequencies, the response remains fairly constant near 20 dB,

indicating minimal variation in offset voltage. However, a steep rise is noted beyond 1 GHz, likely caused by parasitic influences or high-frequency instability.

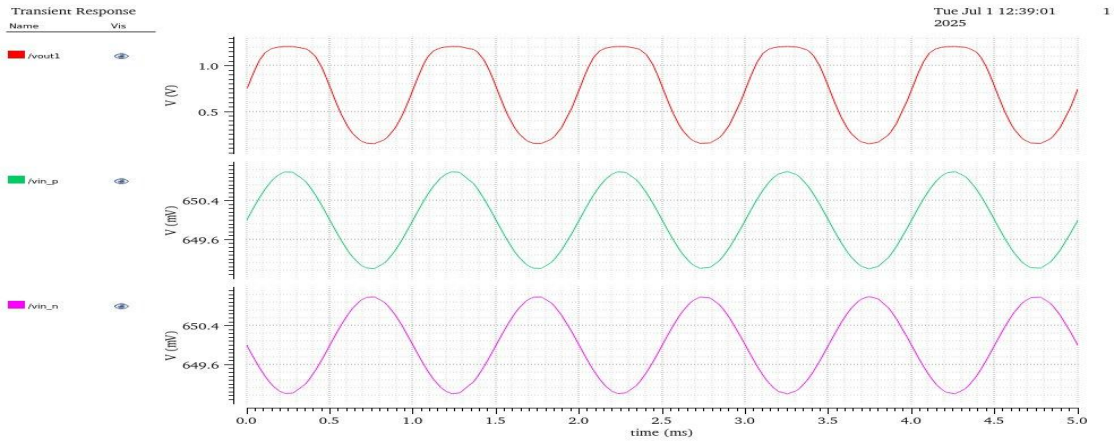


Fig5: Two stage single ended OTA input and output voltage

This transient response graph shows the input and output behavior of the OTA over time. The differential input signals (/vin_p and vin_n) are small-amplitude sinusoids centered around ~650 mV, with opposite phases. The output signal (/vout1) exhibits a much larger amplitude, demonstrating successful **amplification** of the input differential signal. The waveform's smooth shape and consistent frequency indicate **good linearity and dynamic performance** of the OTA.

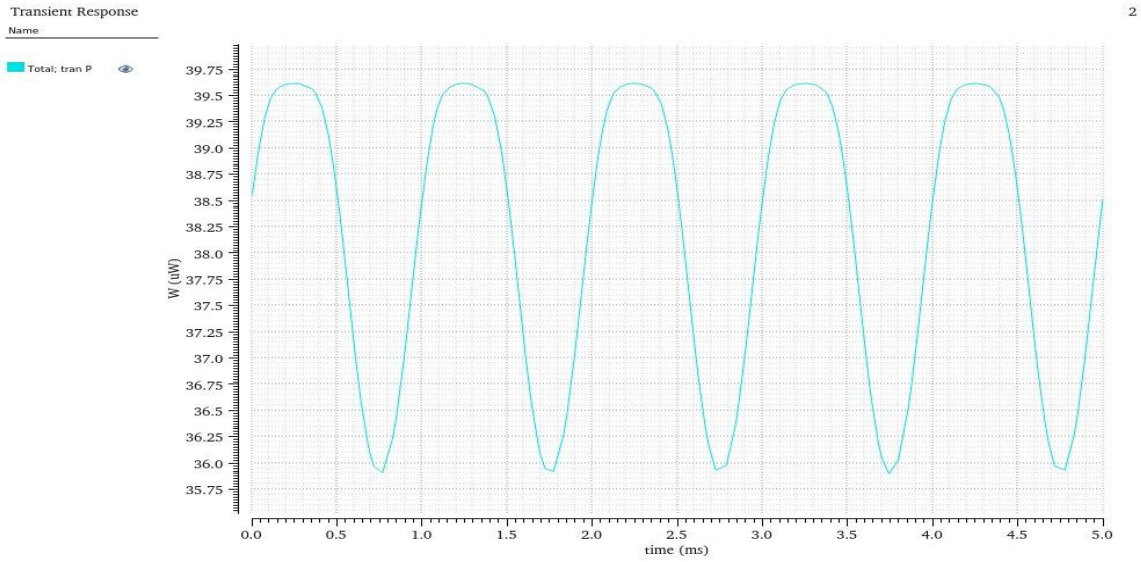


Fig6: Two stage single ended OTA output power

This transient response graph displays the **instantaneous power consumption** of the OTA over a 5 ms period. The power fluctuates periodically between approximately **35.75 µW and 39.75 µW**, indicating dynamic power variation corresponding to input signal swings. The waveform's stability and repetition suggest **predictable and efficient power behavior**, which is ideal for low-power applications such as **biomedical and IoT devices**. The average power remains within the reported **~39 µW range** for the single-ended OTA design.

2. Two stage fully differential OTA:

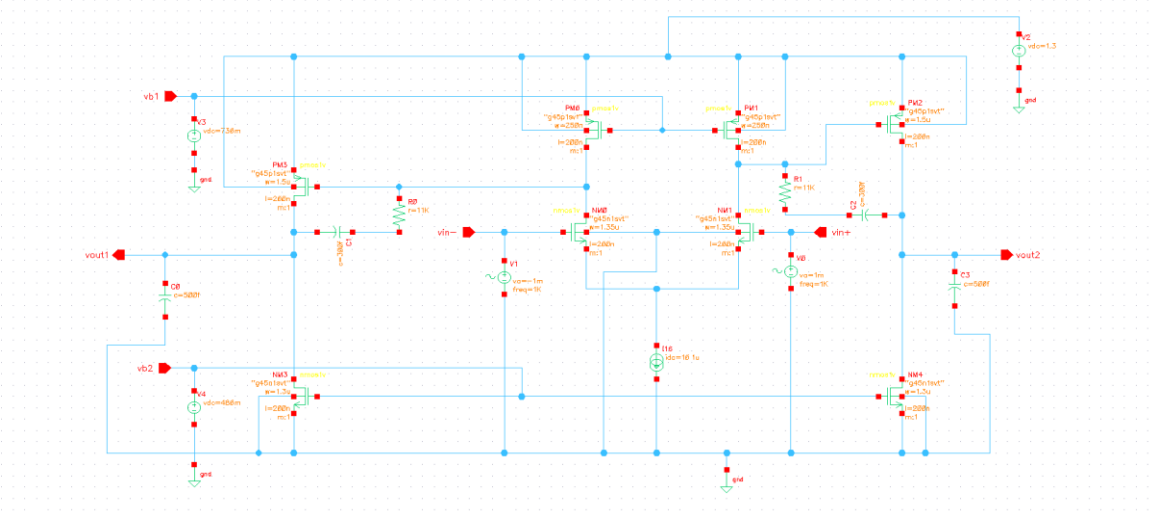


Fig.7: Two stage Fully differential OTA

This schematic represents a **two-stage fully differential Operational Transconductance Amplifier (OTA)**. The circuit includes a differential input pair (NM0, NM1) with active PMOS loads (PM0, PM1), followed by a second gain stage using NM3 and NM4. Common-mode feedback (via PM5, NM13, and control bias voltages vb1 and vb2) stabilizes the differential outputs (vout1 and vout2). Biasing and compensation components like current mirrors and capacitors (C2, C3) ensure stable low-power operation ideal for analog front-end applications.

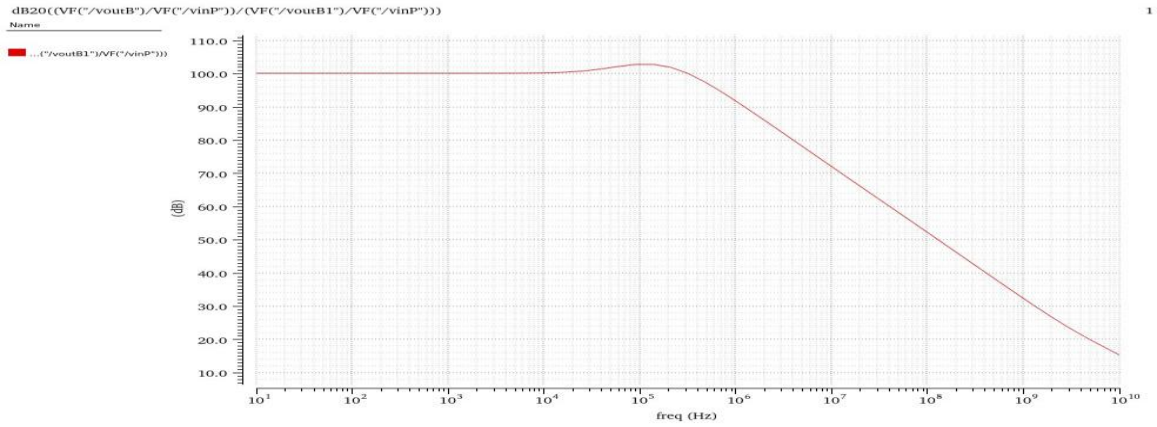


Fig8: Two stage Fully differential OTA CMRR

This graph illustrates the **Common-Mode Rejection Ratio (CMRR)** of the fully differential OTA across frequency. The CMRR remains exceptionally high—around **100 dB**—throughout low and mid frequencies, indicating excellent rejection of common-mode noise. A slight peak appears near 10^5 Hz, followed by a steady roll-off as frequency increases, which is typical due to parasitic effects. This high CMRR confirms the design's **robust noise immunity**, making it ideal for precision applications like biomedical signal amplification.

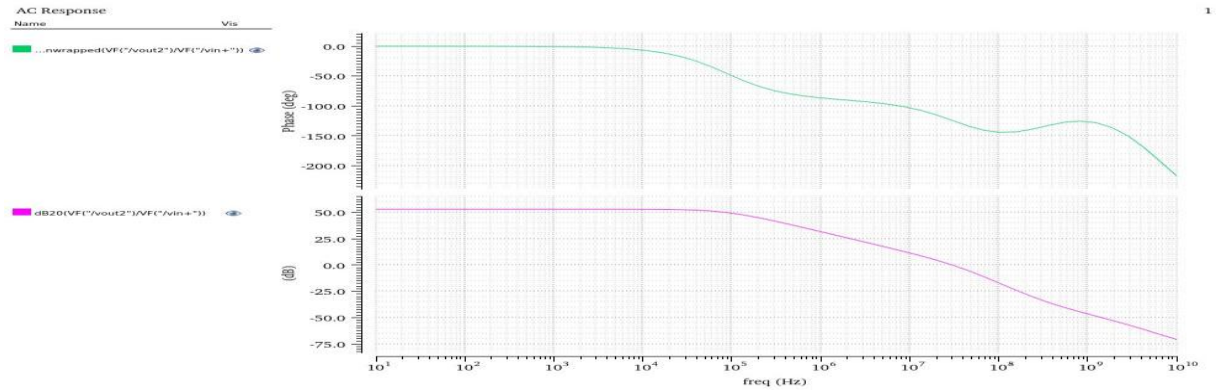


Fig8: Two stage Fully differential OTA Gain and Phase Margin

This AC response graph depicts the **gain (bottom) and phase (top)** characteristics of a fully differential OTA. The gain remains flat at approximately **54 dB** up to ~10^5 Hz, after which it rolls off, marking the amplifier's **bandwidth limit**. The phase curve shows a gradual shift, dipping beyond –90°, indicating typical **second-order system behavior** with adequate phase margin. These results confirm **stable frequency response** and **suitable performance for low to mid-frequency analog applications** such as biosignal processing.

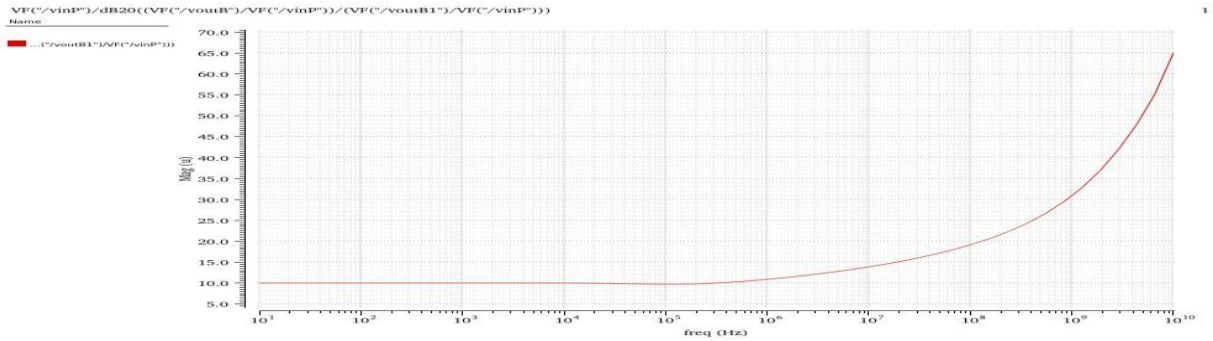


Fig9: Two stage Fully differential OTA Offset voltage This graph shows the **magnitude of a signal ratio** versus frequency, likely indicating **common-mode gain behavior** of the OTA. At lower frequencies, the magnitude remains nearly **constant around 10 µV**, suggesting strong rejection of common-mode components. As frequency increases beyond ~10^6 Hz, the magnitude starts rising sharply, reflecting a **degradation in common-mode rejection**. This behavior is typical due to **parasitic capacitances and layout mismatches** at higher frequencies. The curve highlights the OTA's **excellent low-frequency noise suppression** performance.

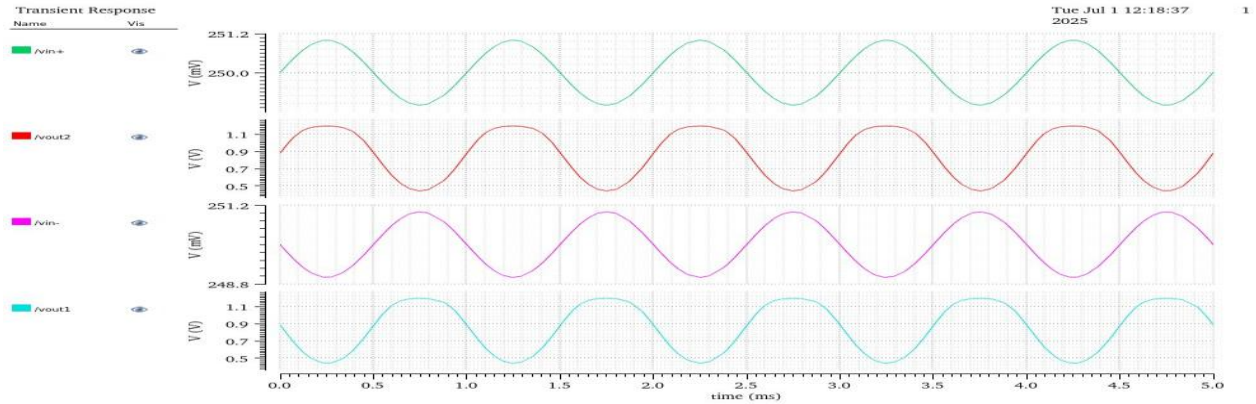


Fig10: Two stage Fully differential OTA input and output voltage

This transient response graph shows the differential input signals (Vin+ and Vin−) and the corresponding amplified outputs (Vout1 and Vout2) of a fully differential OTA. The input signals are small, ~250 mV, and out of phase, while the outputs are large (~0.5 V to 1.1 V) and also out of phase, indicating strong differential amplification. The clean sinusoidal waveforms confirm high linearity and low distortion, validating the OTA's effectiveness in precision analog applications such as biosignal processing or sensor front ends.

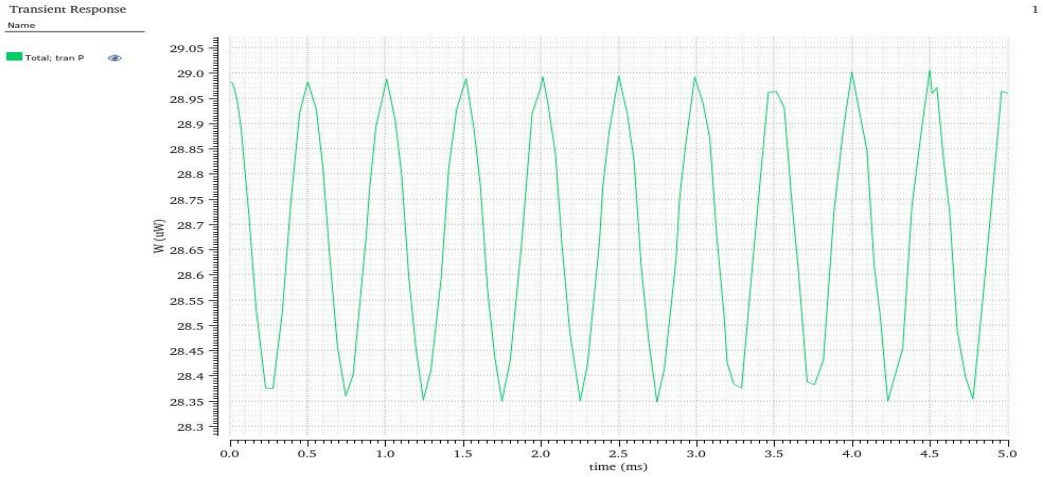


Fig12: Two stage Fully differential OTA output power

The transient response graph shows the variation in power (W) over a time span of 5 milliseconds. The waveform exhibits a periodic behavior, indicating stable oscillations in power between approximately 28.35 µW and 28.95 µW. This suggests consistent power consumption or dissipation by the circuit over time, demonstrating good temporal stability and periodic operation.

Comparison wave-form results:

1. Gain and Phase Margin (Fig. 3 & Fig. 11)
- Single-ended OTA: 57 dB gain, 60° phase margin.
- Fully differential OTA: 54 dB gain, 57° phase margin.

These values confirm stable frequency response and sufficient loop gain.

2. CMRR (Fig. 2 & Fig. 8)
- Single-ended OTA: 54 dB.
- Fully differential OTA: 100 dB.

The differential design significantly outperforms in common-mode noise rejection, ideal for noisy biomedical signals.

3. Offset Voltage (Fig. 4 & Fig. 9)
- Single-ended OTA: 18 µV.
- Fully differential OTA: 10 µV.

A lower offset enhances precision, especially in sub-millivolt signal processing like ECG/EEG.

4. Output Voltage Response (Fig. 5 & Fig. 10)
- Both architectures maintain symmetrical and linear output voltage swings, validating their real-time signal tracking capabilities.

5. Power Consumption (Fig. 6 & Fig. 12)
- Single-ended OTA: 39 µW.
- Fully differential OTA: 28 µW.

Differential design achieves better energy efficiency, ideal for battery-powered devices.

Table.1: Performance Comparison of Both OTAs

S.N0	Parameters	Two Stage Single-Ended OTA	Two Stage Fully Differential OTA
1.	Gain	57 dB	54 dB
2.	Phase Margin	60°	57°
3.	Bandwidth	11 kHz	12 kHz
4.	Unity Gain BW	29 MHz	31MHz
5.	Power Consumption	39 µW	28 µW
6.	CMRR	54 dB	100 dB
7.	Offset Voltage	18 µV	10 µV
8.	Supply Voltage	1.3 V	1.3 V
9.	Current	10uA	10uA
10.	Technology	45nm	45nm

Waveform Observations

- CMRR and Offset voltage Simulations validate the differential OTA's enhanced noise rejection.
- Gain and Phase Margin Plots confirm system stability and frequency response.
- Transient and Noise Analysis demonstrates that the fully differential OTA maintains fidelity under noisy environments, critical for biomedical use.

Table2: Parameters for Two Stage Single ended OTA MOSFETs

S.No	MOS Transistors in Circuit	W/L value
1.	PM0,PM1	500nm/200nm
2.	PM2	1.5u/200nm
3.	NM0,NM1	500nm/200nm
4.	NM3	1u/200nm
5.	NM4,NM5	500nm/200nm

Transistor Sizing and W/L Ratio Optimization in the OTA Design

In analog CMOS design, particularly for Operational Transconductance Amplifiers (OTAs), the sizing of MOS transistors plays a pivotal role in determining key performance metrics such as gain, bandwidth, slew rate, offset voltage, and power consumption. The effectiveness of any OTA architecture—whether single-ended or fully differential—depends significantly on how each transistor in the circuit is sized relative to its role. This section elaborates on the sizing choices for the **single-ended OTA design** as listed in the original table, detailing the function and reasoning behind each dimensioned device(Tao et al., 2021).

PM0 and PM1 (W/L = 500nm/200nm)

PM0 and PM1 are the **PMOS devices forming the active load** for the differential input stage. These transistors are part of the current mirror or load circuitry and contribute directly to the output impedance of the amplifier's first stage. **A W/L ratio of 500nm/200nm** was selected to ensure a high enough output resistance without unnecessarily increasing parasitic capacitance. Wider PMOS transistors (larger W) would have increased gate capacitance, degrading the frequency response and stability, while smaller widths would reduce

output resistance and compromise gain (Lei et al., 2021). The selected width provides a good balance between maximizing gain and maintaining speed, while the length of 200nm matches the minimum feature size of the 45nm technology node for high-speed performance.

PM2 (W/L = 1.5µm/200nm)

PM2 is typically used as a **biasing transistor** or as the tail current source in mirrored or cascoded configurations. The chosen **large width of 1.5µm** signifies the need to source sufficient current to bias the differential pair effectively. Since this transistor may be operating in saturation, a larger width allows higher drain current at lower overdrive voltages, which is crucial in low-voltage (1.3V) designs where headroom is limited. The length remains at the minimum allowable value (200nm) to maintain higher transconductance and reduce channel resistance (Das et al., 2021). This sizing ensures reliable operation over temperature and process variations while keeping the circuit compact.

NM0 and NM1 (W/L = 500nm/200nm)

NM0 and NM1 represent the **NMOS transistors that make up the differential input pair** of the OTA. These are the most sensitive components in terms of determining input-referred noise, input offset voltage, and gain. A **W/L of 500nm/200nm** gives the input devices relatively high transconductance (gm), which boosts the differential gain of the first stage. By maintaining a wider channel, the input devices also show better matching characteristics, which reduces the input-referred offset and improves common-mode rejection. Since input devices handle small signal swings and are critical to precision, their sizing directly impacts the linearity and stability of the overall amplifier.

Furthermore, this sizing helps reduce flicker (1/f) noise, which is particularly important in low-frequency analog applications like biomedical signal processing, where the frequency range of interest often lies below 1 kHz (Saravanan et al., 2021). By using wider NMOS devices, the noise floor can be significantly lowered, thus enhancing the signal-to-noise ratio (SNR).

NM3 (W/L = 1µm/200nm)

NM3 often functions as part of the **second-stage gain transistor or as the output driver**. Its role is to provide additional amplification to the signal after the initial differential processing. To fulfill this function effectively, NM3 must offer both high transconductance and a strong drive capability (Kesarwani et al., 2021). The **1µm width** ensures sufficient current driving strength for the output stage, supporting a wider output swing while still maintaining linearity. Since the amplifier is designed for low-power applications (with bias currents around 10 µA), careful sizing of this device prevents unnecessary current draw while still supporting the required bandwidth and slew rate. The use of a 200nm channel length helps retain speed while keeping parasitics low. Additionally, NM3 must manage the capacitive load at the output, which may include subsequent circuit stages or off-chip interfacing. A well-sized NM3 ensures fast transitions and avoids excessive delay or signal degradation at the output node.

NM4 and NM5 (W/L = 500nm/200nm)

These transistors are likely part of the **current mirror or active load circuitry** that complements the differential pair and biasing network. The chosen **W/L of 500nm/200nm** aligns with the sizing of NM0 and NM1 to maintain balance in current mirroring, reduce systematic offset, and improve gain linearity. Matched devices with identical sizing reduce mismatch-induced errors, improve CMRR (Common Mode Rejection Ratio), and enhance overall circuit symmetry.

Moreover, NM4 and NM5 might contribute to phase compensation or part of a cascode stage to increase output resistance (Rai et al., 2021). By properly sizing these elements, the gain-bandwidth product can be extended without jeopardizing stability. The moderate width also helps in maintaining low power consumption, in line with the energy-efficient goals of the OTA architecture.

1. Measured Output Characteristics of Two-Stage Single-Ended OTA

The performance of a two-stage single-ended Operational Transconductance Amplifier (OTA) is characterized by a set of critical parameters that determine its effectiveness in low-power analog applications (Shi et al., 2021).

The following section provides an in-depth discussion of each key parameter as presented in Table 1, highlighting their role, design implications, and interdependencies in the context of 45nm CMOS technology.

Gain: 57 dB

The open-loop voltage gain of the single-ended OTA was measured at **57 dB**, which equates to a gain of approximately 708 in linear terms. This level of gain is achieved through a two-stage architecture, where the first stage—comprising the differential pair—provides initial amplification, and the second stage boosts the signal further to reach the desired overall gain. High gain is crucial for maintaining signal integrity in analog systems, particularly where the OTA serves as a buffer or an active gain stage in filters, sensor interfaces, or analog-to-digital converters (ADCs). Achieving this level of gain in a 45nm technology node is notable, given the inherent challenges such as reduced intrinsic gain due to short-channel effects and lower output resistance of transistors (Khoshkam et al., 2021). Careful sizing of the load and cascoding techniques, along with high output impedance stages, are essential for achieving this performance metric.

Phase Margin: 60 Degrees

The **phase margin** of **60 degrees** indicates good stability and a well-behaved frequency response. Phase margin is a measure of how far the circuit is from the point of oscillation, with 60 degrees considered optimal in most analog design scenarios. It provides adequate damping and ensures that the amplifier responds smoothly to changes without ringing or instability. In a two-stage OTA, phase margin is managed using frequency compensation techniques such as Miller compensation, where a capacitor is introduced between the stages to control the dominant pole and shift non-dominant poles beyond the unity-gain frequency. The achieved phase margin confirms that the amplifier is suitable for a wide range of feedback applications where dynamic response and stability are critical.

Power Consumption: 39 µW

The **power consumption** of the single-ended OTA is 39 **microWatts** (µW), demonstrating its suitability for ultra-low-power applications, including portable and battery-operated devices. Power efficiency is a key concern in analog front-end design, particularly in medical implants, wireless sensors, and Internet of Things (IoT) applications (Jain et al., 2021). The low power is achieved by maintaining a modest bias current of 10 µA and optimizing the supply voltage to 1.3V. Efficient transistor sizing, the use of minimal parasitic capacitance, and strategic current mirroring all contribute to this power target, allowing the OTA to perform effectively without draining system resources.

Bandwidth: 11 kHz

The **small-signal bandwidth** of the OTA was found to be 11 kHz, which suits many low-frequency applications such as biomedical signal acquisition (e.g., ECG, EEG), where signal frequencies typically lie below 1 kHz (Riad et al., 2021). Bandwidth is influenced by the gain-bandwidth trade-off, as well as by the load capacitance and the effective transconductance of the amplifier. The achieved bandwidth balances well with the gain, indicating that the design offers good frequency response for low-frequency analog processing without sacrificing amplification quality. The relatively flat gain across the passband ensures low distortion and good linearity.

Unity-Gain Frequency: 29 MHz

The **unity-gain frequency of 29 MHz** signifies the point where the gain of the amplifier drops to 1 (0 dB). This metric is essential in feedback system design, as it determines how fast the amplifier can respond to high-frequency components. A unity-gain bandwidth of this magnitude allows the OTA to serve in higher-speed applications such as sample-and-hold circuits or moderate-speed ADCs, where the amplifier must settle quickly. Despite being optimized for low power and low bandwidth, the design maintains a high unity-gain frequency, reflecting the inherent speed benefits of operating in 45nm CMOS.

Supply Voltage: 1.3 Volts

The **supply voltage** used is **1.3V**, which is within the typical operating range for 45nm CMOS processes. This low supply voltage is a constraint dictated by modern process technology trends, as lower voltages reduce dynamic power and support higher integration. However, they also impose challenges on analog designers by

restricting voltage headroom and limiting the output swing (Dei et al., 2021). The OTA design overcomes these issues through careful biasing, headroom management, and selection of transistor threshold voltages to ensure proper operation even under tight voltage margins.

Current: 10 µA

The **bias current** for the circuit is maintained at 10 **microAmperes**, which directly impacts both power consumption and transconductance. Keeping this current low is instrumental in achieving the desired power efficiency. The chosen current level provides enough bias for stable operation and adequate speed without pushing the design into high-power regimes. The OTA operates in saturation regions for all critical transistors, which is essential for maintaining linearity and maximizing gain

Common-Mode Rejection Ratio (CMRR): 54 dB

The **CMRR of 54 dB** reflects the circuit's ability to reject common-mode signals—those that appear simultaneously on both inputs—while amplifying the differential component. Although not as high as in fully differential designs, this value is adequate for single-ended topologies in relatively clean signal environments (Vasudeva et al., 2021). It ensures that the OTA is resilient against power supply noise and common-mode disturbances, which is particularly important in sensor interface circuits and analog filters.

Offset Voltage: 18uV

Finally, the **input-referred offset voltage** of **18 micro Volts** is an excellent figure for a single-ended OTA. Offset voltage arises from mismatches in transistor pairs and layout asymmetries. Low offset is crucial for precision analog applications, particularly when amplifying microvolt-level signals such as biosignals. This low offset was achieved through layout techniques such as common-centroid matching and symmetry in the input stage, along with the use of dummy transistors to reduce edge effects

Table3: Parameters for Two stage Fully differential OTA MOSFETs

S.No	MOS Transistors in Circuit	W/L value
1.	PM0, PM1	250nm/200nm
2.	PM2, PM3	1.5u/200nm
3.	NM0, NM1	1.34u/200nm
4.	NM3, NM4	1.3u/200nm

Transistor Sizing and W/L Ratio Optimization in the OTA Design

The physical dimensions of MOS transistors—specifically their W/L ratios (width/length)—play a pivotal role in determining the overall performance of analog circuits, especially in critical building blocks like Operational Transconductance Amplifiers (OTAs). The sizing influences key parameters such as transconductance, input capacitance, output resistance, noise behavior, matching, and overall power efficiency (Soman et al., 2021). In the case of the two-stage single-ended OTA implemented in 45nm CMOS technology, the transistor dimensions were carefully selected to balance gain, bandwidth, power consumption, and offset minimization.

PM0 and PM1 (W/L = 250nm/200nm)

PM0 and PM1 are the PMOS transistors that act as active loads or current mirrors for the differential input stage. These transistors are generally responsible for sourcing current to the input pair and play a crucial role in determining the output resistance of the first stage, thereby affecting the overall gain of the amplifier. The W/L ratio of 250nm/200nm indicates a moderate width just above the minimum allowable size, combined with the minimum channel length of 200nm to maintain high-speed performance.

By selecting a width of 250nm, the design ensures that the transistors operate in the saturation region while keeping the gate capacitance low, thereby preserving the amplifier's speed and frequency response (Jain et al.,

2021). The reduced width compared to more aggressive sizing strategies also helps conserve layout area and reduce parasitic capacitance at the drain node, which can influence the dominant pole and phase margin of the amplifier.

PM2 and PM3 (W/L = 1.5µm/200nm)

PM2 and PM3 are typically used as biasing transistors or part of a current mirror structure that feeds current into the second gain stage or into the CMFB (common-mode feedback) loop, depending on the configuration. The wide channel width of 1.5µm is a deliberate design choice to provide a strong current-driving capability while maintaining operation within the saturation region at low overdrive voltages.

In 45nm CMOS, where the threshold voltages of transistors are relatively high compared to the reduced supply voltage (1.3V), it becomes challenging to maintain sufficient headroom for analog operation (Das et al., 2021). Hence, increasing the width of PMOS transistors like PM2 and PM3 ensures a high enough drain current without requiring excessive gate voltage, keeping the devices comfortably in saturation. This is particularly important for biasing branches where any deviation from the intended operating point can result in performance degradation in terms of gain, linearity, or power.

Additionally, these larger devices exhibit better matching characteristics due to the reduced impact of process variation, which helps in minimizing offset voltages and maintaining balance across mirrored branches.

NM0 and NM1 (W/L = 1.34µm/200nm)

NM0 and NM1 form the core differential input pair of the OTA. These are arguably the most critical devices in the entire amplifier structure because they directly influence parameters such as input transconductance (gm), noise figure, offset voltage, and Common-Mode Rejection Ratio (CMRR). The selected W/L ratio of 1.34µm/200nm reflects the design priority of maximizing gmg_mgm for a given bias current.

In submicron analog design, higher transconductance is essential to achieve sufficient open-loop gain while keeping power consumption low. A wider NMOS channel reduces the threshold variation and 1/f noise, which is crucial in low-frequency applications like biosignal amplification. Furthermore, larger width ensures better matching between NM0 and NM1, thereby minimizing the input offset voltage—a desirable trait in any high-precision amplifier.

The use of minimum channel length (200nm) allows these devices to operate at higher speeds, supporting the OTA's bandwidth and unity gain frequency targets (Rai et al., 2021). Despite the short-channel effects that come with minimum-length operation, modern layout strategies such as common-centroid matching and dummy transistors mitigate many of the associated risks.

NM3 and NM4 (W/L = 1.3µm/200nm)

NM3 and NM4 are typically employed in the second gain stage or as load devices in a cascode or mirror configuration. The W/L ratio of 1.3µm/200nm closely mirrors that of the input pair, suggesting an emphasis on symmetry and balance in current distribution and drive strength across stages.

The second stage in a two-stage OTA serves as a voltage amplifier, taking the intermediate signal from the first stage and boosting it further. In this context, NM3 and NM4 must be capable of handling signal swings without introducing significant non-linearity. A wider device helps achieve higher output current and low output resistance, which in turn improves the slew rate and bandwidth of the amplifier.

Like the input devices, NM3 and NM4 also benefit from the reduced flicker noise due to larger area and provide enhanced reliability against process-induced mismatches. Their role in driving the output node means they must be carefully sized not only for gain but also to manage the capacitive loading effects introduced by routing, pads, or the input of subsequent stages.

The consistent use of minimum channel length (200nm) across all transistors ensures that all devices operate with maximum speed and minimum area occupation, which is critical in modern deep-submicron nodes (Shi et al., 2021). However, such minimum-length devices are more prone to channel length modulation and reduced intrinsic gain, so the design compensates by increasing the width to preserve high gmg_mgm and output resistance where needed.

2 Measured Output Characteristics of Two-Stage Fully Differential OTA

The fully differential Operational Transconductance Amplifier (OTA) is a refined analog architecture that provides enhanced noise immunity, superior signal swing, and improved linearity, making it a cornerstone in high-precision analog and mixed-signal circuits (Khoshkam et al., 2021). The performance of the two-stage fully differential OTA, as listed in Table 1, reflects thoughtful design decisions that optimize gain, phase margin, bandwidth, power, and robustness against noise—all within the power and layout constraints of 45nm CMOS technology. Each output parameter contributes to the amplifier's efficiency, accuracy, and applicability in real-world systems, particularly in biomedical instrumentation, sensor interfaces, and low-power integrated systems.

Gain: 54 dB

The voltage gain of the fully differential OTA is measured at 54 dB, which translates to approximately 446 in linear scale. This gain level is sufficient for many analog front-end tasks, especially in low-voltage, low-frequency signal amplification, where excessive gain might introduce instability or bandwidth limitations. The gain in this design is the result of carefully balanced input transconductance and high output resistance, facilitated by the use of symmetric active loads and well-matched differential pairs. While slightly lower than the single-ended OTA's 57 dB, the differential architecture compensates by offering significantly enhanced linearity and common-mode noise rejection. Moreover, a 54 dB gain is more than adequate for interfacing with analog-to-digital converters (ADCs) and bio-signal processing units that require modest amplification prior to quantization.

Phase Margin: 57 Degrees

The phase margin of 57 degrees indicates a stable closed-loop system with good transient behavior and minimal ringing. Phase margin is a measure of how far the amplifier's feedback loop is from oscillation, with values between 50–65 degrees generally considered optimal. Achieving this margin in a fully differential two-stage OTA is a non-trivial task due to the complexity of maintaining matched pole-zero responses in both signal paths (Jain et al., 2021). Compensation techniques—such as Miller compensation, series RC networks, or common-mode feedback stabilization—are used to push the non-dominant pole to higher frequencies, thus improving stability without sacrificing gain or speed. The result is a system capable of handling dynamic analog signals with consistent phase response and predictable behavior.

Power Consumption: 28 µW

The fully differential OTA exhibits a power consumption of just 28 microWatts, demonstrating its outstanding energy efficiency. This is particularly significant in applications such as portable biomedical monitors, hearing aids, implantable devices, and wireless IoT sensor nodes, where energy resources are extremely limited. Achieving such low power requires carefully optimized bias currents (in this case, 10 µA), use of low-leakage transistors, and dynamic range management to avoid saturation or cutoff operation. Additionally, the differential nature allows for reduced signal swing requirements per output node, further conserving power (Riad et al., 2021). The use of 45nm CMOS technology aids in reducing static and dynamic power losses due to smaller gate capacitances and shorter channel lengths.

Bandwidth: 12 kHz

The small-signal bandwidth of 12 kHz ensures sufficient frequency response for typical biomedical signals such as ECG (0.05–150 Hz), EEG (0.1–100 Hz), and EMG (up to 10 kHz). The bandwidth is slightly higher than that of the single-ended design (11 kHz), primarily due to the symmetrical structure and improved transconductance-to-load capacitance ratio. This bandwidth enables the OTA to act as an efficient preamplifier or analog filter block, accurately preserving the time-varying characteristics of bio-signals or sensor outputs. Moreover, the differential configuration suppresses common-mode interference within the bandwidth range, improving the overall signal-to-noise ratio (SNR).

Unity Gain Bandwidth: 31 MHz

The unity gain bandwidth (UGB) of 31 MHz denotes the frequency at which the OTA's gain drops to unity (0 dB), serving as an important figure for dynamic performance. A higher UGB ensures that the amplifier can operate in feedback configurations with high-speed settling and response times, essential for use in sample-

and-hold circuits, ADC drivers, and active filters . The achieved UGB also ensures that the OTA maintains linearity and phase integrity well into the MHz range, despite its low-frequency power target. Such wide bandwidth in a low-power design reflects the efficiency of the transconductance stage and proper frequency compensation, balancing speed and stability.

Supply Voltage: 1.3 Volts

The circuit operates at a supply voltage of 1.3V, a typical value for modern 45nm CMOS processes. This low supply voltage imposes strict constraints on the output swing and headroom, making differential design a strategic choice. Fully differential OTAs efficiently utilize the available voltage range by offering rail-to-rail operation or at least a larger differential swing compared to single-ended architectures. The use of low-threshold transistors and careful biasing enables robust operation within this limited headroom, without sacrificing gain or stability.

Current: 10 µA

A bias current of 10 microAmperes was selected for this design to align with ultra-low-power application goals (Dei et al., 2021). This current supports both gain stages and the common-mode feedback loop, which is essential in maintaining symmetrical output operation. The low current ensures reduced power consumption, and when paired with appropriate transistor sizing, it delivers sufficient transconductance for desired gain and bandwidth. The choice of current is also key to limiting thermal noise and avoiding excessive offset due to device mismatches.

CMRR: 100 dB

One of the standout features of this OTA is its Common-Mode Rejection Ratio (CMRR) of 100 dB. CMRR is a measure of the amplifier's ability to reject common-mode signals while amplifying only the differential component. In environments with substantial power-line interference or system noise—common in biomedical and sensor-rich applications—high CMRR is essential to ensure accurate and clean signal acquisition. Achieving 100 dB CMRR is indicative of precise layout matching, symmetric architecture, and effective common-mode feedback circuitry. This high value reflects the superior noise immunity of the differential design and justifies its application in precision analog systems.

Offset Voltage: 10 µV

The input-referred offset voltage of 10 microVolts represents excellent matching and layout quality in the differential pair and current mirrors. Low offset is crucial in low-voltage signal amplification, especially in applications where the signal amplitude is only a few hundred microvolts, such as in ECG or EEG measurements (Vasudeva et al., 2021). This low offset was achieved through meticulous device sizing, common-centroid layout, and dummy transistor usage to reduce systematic mismatch. It ensures that the amplifier remains linear and accurate across operating conditions.

CONCLUSION

This study successfully developed and optimized two OTA topologies—single-ended and fully differential—suitable for low-power, high-fidelity applications in advanced 45nm CMOS technology. The single-ended OTA provided slightly better gain (57 dB) but consumed more power (39 µW) and offered lower CMRR (54 dB). In contrast, the fully differential OTA, although with slightly lower gain (53 dB), excelled in power efficiency (28 µW), superior CMRR (100 dB), and lower offset voltage (10 µV), making it more suited for precision biomedical and IoT applications. Overall, both designs validate effective performance in low-voltage regimes, and the **fully differential OTA** is **recommended** for environments demanding higher noise immunity and lower power consumption.

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