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Implementation Of Low Power And High-Speed Adders Using Different Techniques

Pilla Bhaskar Rao[1*], Nishant Kumar[2]
[1,2] Department of Electronics and Communication Engineering, Koneru Lakshmaiah Education Foundation, Andhra Pradesh, India-522302
Email: pillabasi1245@gmail.com[1*], nishantkumar@kluniversity.in[2]

ABSTRACT *- Addition is an important operation among all the fundamental operations of calculations, used for many arithmetic and logical calculations. This project's objective is to reduce power and delay by employing various techniques like CMOS design, TGFA (Transmission Gate Full Adder), SERF (Static Energy Recovery Full Adder) methods that are used for extending the battery life. Using different techniques of full adder, the 16-bit Ripple Carry Adder (RCA) and 16-bit Carry Select Adder (CSA) designs are implemented. The timing parameters of each adder were first characterized. Comparing the conventional adders in various performances such as power consumption and speed. The adders' designs are made and implemented using Tanner EDA v14.1 with 130nm and 90nm technologies.*
Keywords *- Full Adder, TGFA (Transmission Gate Full Adder), Ripple Carry Adder (RCA), Carry Select Adder (CSA), SERF (Static Energy Recovery Full Adder)*

1. INTRODUCTION

Very Large-Scale Integration (VLSI) deals with design, fabrication and application of Integrated circuits (IC) or microchips containing millions of transistors. These transistors are densely packed onto a single chip, enabling the creation of complex electronic systems on a small silicon wafer. The evolution of VLSI technology is the basis for the advancement of modern electronics, allowing the advancement of smaller, faster, and more efficient electronic devices like smartphones, computers, and medical equipment. The applications of Very Large-Scale Integration (VLSI) include audio processing, video processing, Graphical Processing Unit (GPU), Arithmetic logic unit (ALU) of CPUs of computers, microprocessors, digital signal processors and data processors using Arithmetic and logical operations. Formerly, VLSI applications are dependent on area, cost and reliability instead of power. Of late, the growing demand for usage of electronic devices such as portable mobile phones and laptops is leading to high power consumption. This creates reduced battery life and device failures. In order to control the heat levels, cooling arrangements are required for the devices with high power consumptions. So, nowadays the semiconductor industries seeks to design the devices with low powers and higher speed.

Power consumption in VLSI circuits is caused majorly due to dynamic, static and short circuit power consumption. Dynamic power consumption arises due to the charging and discharging of capacitor loads during transistor switching. It can be reduced by optimizing circuit design,
minimizing switching activity and lowering the supply voltage. Static power consumption arises due to sub threshold leakage currents in transistors. Techniques such as power gating, transistor sizing, and threshold voltage scaling are used to mitigate static power consumption. Short circuit power dissipation occurs when both the PMOS transistor and NMOS transistor in a CMOS circuit are simultaneously conducting. Design techniques such as transistor sizing and circuit restructuring help mitigate short-circuit power.

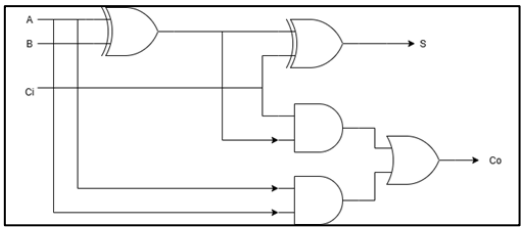
2. PROPOSED DESIGNS FOR ADDER

Here comparative analysis is made by considering different 1-bit full adder designs, namely 10T TGFA design, 28T CMOS, 10T SERF design. Design of 16-bit Carry Select Adder (CSA), 16-bit Ripple Carry Adder (RCA) by using 28T CMOS, TGFA, SERF full adders with 130nm and 90nm.

2.1. A BASIC FULL ADDER DESIGN

Designing of a basic full adder requires the use of three single bits for input and consideration of the output as sum and carry. The basic model of a full adder with the equation is shown below.

Sum = {A xor B xor Cin}
Carry = {((A xor B) and Cin) or (A and B)}
Figure 1. Full Adder's block diagram



2.2. 28T CMOS 1-BIT FULL ADDER DESIGN

The combinations of PMOS and NMOS transistors are used to design 28T CMOS full adder. It consists of 28 transistors. It has low power consumption and delay compared to basic full adder because the transistor count is reduced in 28T CMOS full adder than basic full adder. The major setback of this design is use of many transistors. This leads to dynamic power consumption and increase in delay. The specifics of the implementation, including transistor sizing, connectivity and the overall architecture. The design is shown below.

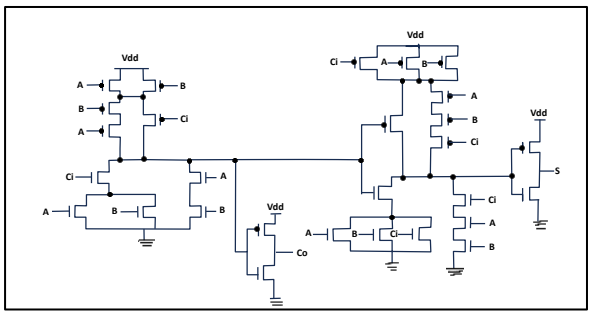


Figure 2. 28T CMOS Full adder block diagram

2.3. 10T TGFA 1-BIT FULL ADDER DESIGN

A transmission gate full adder (TG full adder) logic design is needed to implement the design using XOR and XNOR gates and it consists of 10 transistors. It is based on transmission gates, and it is designed for low power dissipation. This is smaller in terms of size when compared to a 28T design and requires less power, area and the delay. TG full adder design has no direct path for ground leads to low power. The goal in using transmission gates is often to achieve a balance between speed, area and power consumption in digital circuits design. The design is shown below.

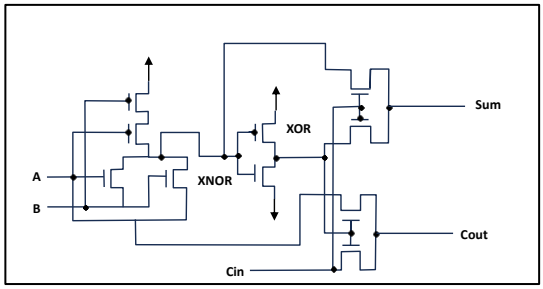


Figure 3. 10T TGFA Full Adder block Diagram

2.4. 10T SERF FULL ADDER DESIGN

The SERF Full adder logic design is implemented by the design with XOR and XNOR gates. It is mainly designed to reduce the static power dissipation in digital circuits. It requires just 10 transistors to implement a full adder design, and this circuit works well with higher supply voltages. The reduction in power consumption is due to no direct ground path. The design is shown in figure below.

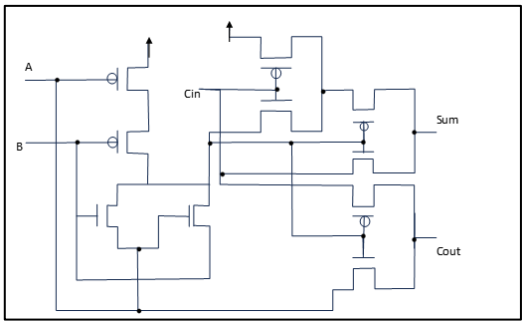


Figure 4. 10T SERF full adder block diagram

2.5. RIPPLE CARRY (RC) ADDER DESIGN

Ripple Carry Adder is designed by series cascading full adder blocks which contain individual full adder cells. Then the carry created is sent on to the respective adder cells. The result calculation takes place only after the carry from the previous stage is given as an input to present stage. This carry output of each full adder is present as input to its next full adder which results in longer propagation delays compared to other adder architectures. Initially we design 4-bit ripple carry adder by 28T, TG, SER full adders and then designing of a 16-bit ripple carry adder by using a 4-bit ripple carry adder. The design is given below figure.

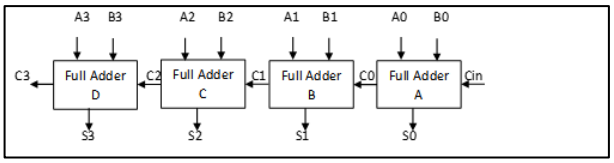


Figure 5. 4-bit ripple carry adder block diagram

2.6. CARRY SELECT ADDER DESIGN

Carry select adder is fastest adder. Generally, it consists of Ripple Carry Adders and a Multiplexer. The main idea is to precompute the sum and carry for each block with carry-in 0 as well as carry-in 1, two adders are required for each block except first one. After the two results are obtained, the corrected sum, and the corrected carry-out is then selected using the Multiplexer. Initially designing of 4-bit Carry Select Adder by using the techniques of 28T, TG, SER full adders, then designing of 16-bit Carry Select Adder by using a 4-bit Carry Select Adder. The design is given below.

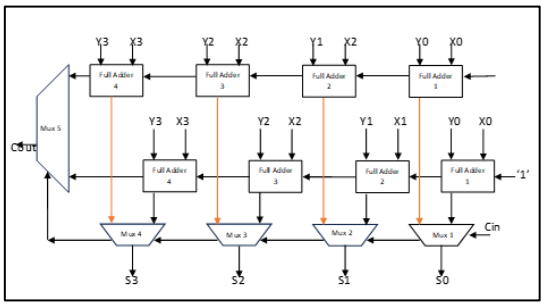


Figure 6. 4-bit carry select adder block diagram

3. SIMULATION RESULTS

3.1. Design of a 28T CMOS Full Adder Using Tanner EDA S_Edit

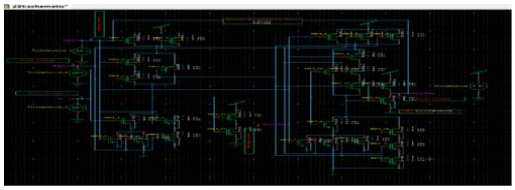


Figure 7. 28T CMOS 1-bit Full Adder Schematic Diagram

The length and width of the transistor for 130nm technology is 0.13um and 0.52um. For 90nm technology the length and width of the transistor is 0.09um and 0.36um respectively. The output wave forms shown in below.

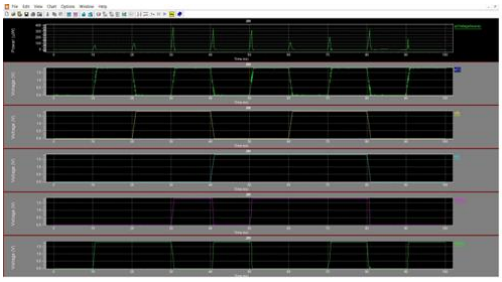


Figure 8. Output of 28T CMOS 1-bit Full adder

3.2. 10T TG Full Adder Design Using Tanner EDA S_Edit

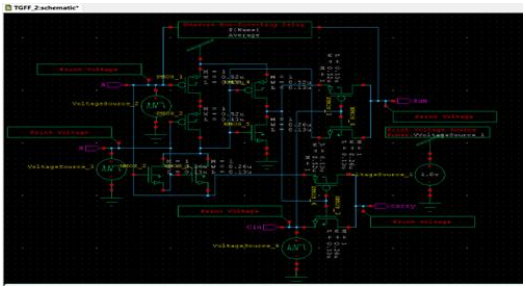


Figure 9. 10T TGFA 1-bit Full Adder schematic diagram

The schematic design of 10T TGFA 1-bit full adder using Tanner EDAV14.1 130nm and 90nm technology. The length and width of the transistor for 130nm technology is 0.13um and 0.52um. For 90nm technology the length and width of the transistor is 0.09um and 0.36um respectively. The output wave forms shown below fig 10.

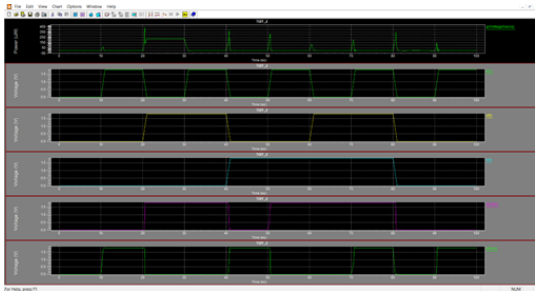


Figure 10. Output of 10T TGFA 1-bit Full adder

3.3. 10T SERF Full Adder Design using Tanner EDA S-Edit

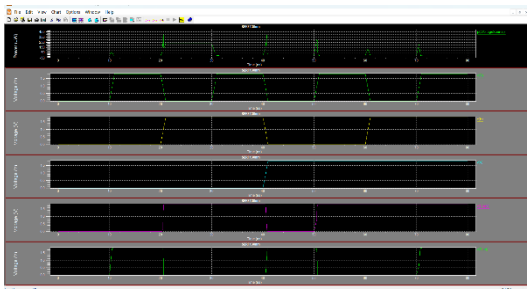


Figure 11. Schematic of 10T SERF 1-bit Full adder

The length and width of the transistor for 130nm technology is 0.13um and 0.52um. For 90nm technology the length and width of the transistor is 0.09um and 0.36um respectively. The output wave forms are shown below.

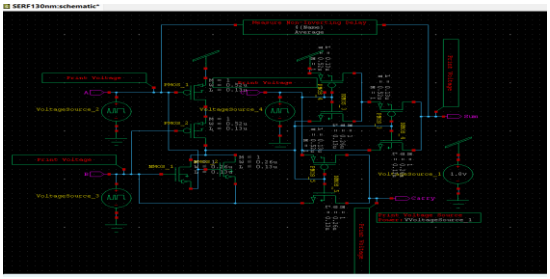


Figure 12. Output of 10T SERF 1-bit Full adder

3.4. Ripple Carry Adder Design using Tanner EDA S-Edit

The schematic designs of both 130nm and 90nm technologies of 28T CMOS,10T TG,10T SERF 4-bit Ripple Carry Adders are converted into symbols to generate 16-bit Ripple Carry Adders of 28T CMOS,10T TG,10T SERF techniques.

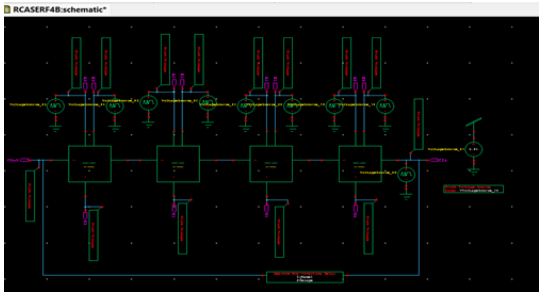


Figure 13. 10T 4-bit Ripple carry adder schematic diagram

The schematic design of 4-bit 10T SERF Ripple Carry Adder using Tanner EDAV14.1 130nm and 90nm technology. The output shown in below is the figure.

Figure 14. output of 10T 4-bit ripple carry adder

By substituting the symbols of 4-bit Ripple Carry Adders of 28T CMOS,10T TG Full Adders of both 130nm and 90nm technologies in above figure generates the schematic design of 16-bit 28T CMOS,10T TGFA Ripple Carry Adder using Tanner EDAV14.1 130nm and 90nm technologies

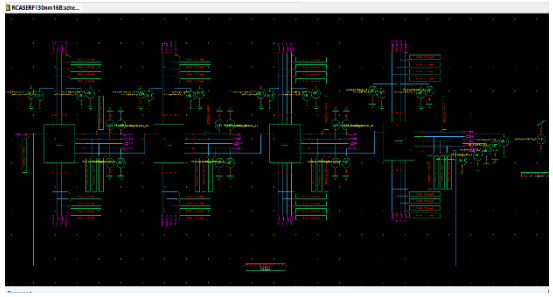


Figure 15. Schematic of 10T SERF 16-bit Ripple carry adder

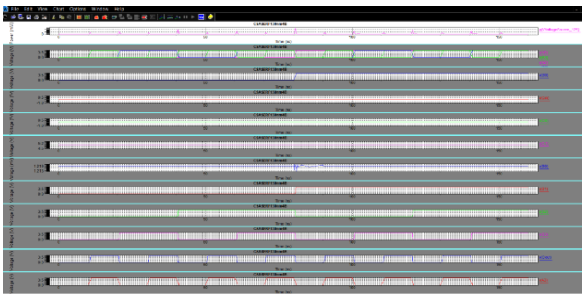


Figure 16. Output of 16-bit 10T SERF Ripple carry adder

By substituting the symbols of 4-bit Ripple Carry Adders of 28T CMOS,10T TG Full Adders of both 130nm and 90nm technologies in above figure generates the schematic design of 16-bit 28T CMOS,10T TGFA Ripple Carry Adder using Tanner EDAV14.1 130nm and 90nm technologies.

3.5. Carry Select Adder Design using Tanner EDA S-Edit

The schematic design of 4-bit 10T SERF Carry Select Adder using Tanner EDAV14.1 130nm and 90nm technology. The output is shown below.

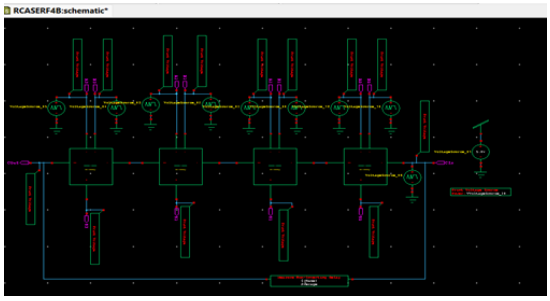


Figure 17. Schematic of 10T SERF 4-bit Carry select adder

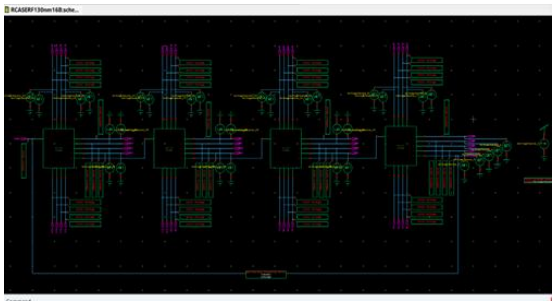


Figure 18. Output of 10T SERF carry select adder

The schematic of 16-bit 10T SERF Carry Select Adder using Tanner EDAV14.1 130nm and 90nm technology. The output is shown below.

Figure 19. Schematic of 10T SERF 16-bit carry select adder

Figure 20. Output of 10T SERF 16-bit carry select adder

Comparative analysis of CMOS 28T full adder, 10T TG full adder, 10T SER full adders and Ripple Carry Adder and Carry Select Adders' area, power and delay are shown in the Tables below.

TABLE I. Comparison Of 1-Bit Full Adder Of 130nm,90nm Power, number of Transistors used and Delay.

		Power consumption (uw)	N0 of Transistors used	Delay(Gs)
28T CMOS	4 Bit	3.92	28*4	1.23
	16 Bit	15.4	28*16	1.23
10T TGFA	4 Bit	0.0187	10*4	1.23
	16 Bit	1.87	10*16	1.23
10T SERF	4 Bit	0.00018	10*4	1.23
	16 Bit	0.18	10*16	1.23

TABLE II Comparison Of 130nm Ripple Carry Adder Power, number of Transistors used and Delay.

		Power consumption (uw)	N0 of Transistors used	Delay(ns)
28T CMOS	130nm	7.32	28	45.10
	90nm	1.65	28	1.9
10T TGFA	130nm	2.51	10	39.9
	90nm	1.49	10	0.41
10T SERF	130nm	1.85	10	0.328
	90nm	0.72	10	0.302

TABLE III Comparison Of 90nm Ripple Carry Adder Power, number of Transistors used And Delay

		Power consumption (uw)	N0 of Transistors used	Delay(Gs)
28T CMOS	4 Bit	526.25	28*4	1.23
	16 Bit	2031.12	28*16	1.23
10T TGFA	4 Bit	5.12	10*4	1.23
	16 Bit	453.6	10*16	1.23
10T SERF	4 Bit	0.36	10*4	1.23
	16 Bit	4.12	10*16	1.23

TABLE IV Comparison Of 130nm Carry Select Adder Power, number of Transistors used And Delay

		Power consumption (uw)	N0 of Transistors used	Delay(Gs)
28T CMOS	4 Bit	1187.23	28*4	0.617
	16 Bit	9638.41	28*16	0.617
10T TGFA	4 Bit	1033.3	10*4	0.617
	16 Bit	5860.4	10*16	0.617
10T SERF	4 Bit	485.5	10*4	0.617
	16 Bit	3084.6	10*16	0.617

TABLE V Comparison Of 90nm Carry Select Adder Power, number of Transistors used And Delay

		Power consumption (uw)	N0 of Transistors used	Delay(Gs)
28T CMOS	4 Bit	10.5	28*4	0.617
	16 Bit	67.9	28*16	0.617
10T TGFA	4 Bit	9.8	10*4	0.617
	16 Bit	37.9	10*16	0.617
10T SERF	4 Bit	4.5	10*4	0.617
	16 Bit	19.1	10*16	0.617

From the above analysis SERF technique has better performance in both 130nm and 90nm technologies

4. CONCLUSION AND FUTURE SCOPE

This project used various circuit design techniques to design and analyze 4-bit and 16-bit ripple carry adders. Tanner EDA tools were used to assess performance metrics like power consumption and propagation delay at 90 nm and 130 nm technology nodes, with supply voltages of 1.0 V and 1.8 V. In comparison to other conventional and transistor-level designs, the 10T SERF (Static Energy Recovery Full Adder) technique was found to produce the most efficient results, with lower power consumption and reduced delay. This efficiency is achieved because the SERF design minimizes switching activity and reuses charge, thereby lowering dynamic power dissipation. Additionally, using fewer transistors in the design can greatly lower the adder circuits' leakage power, which directly leads to a more compact and energy-efficient implementation.

In the future, the design process can be expanded to further optimize the fundamental components. For example, ultra-low transistor count designs like 8T or 6T structures can be used to implement 1-bit full adders, further reducing area and power requirements while maintaining a respectable speed. Higher-order adders, including 32-bit, 64-bit, and even 128-bit ripple carry adders, can be built at the system level by cascading these optimized full adder cells. Furthermore, to enhance overall performance in terms of delay, power, and area efficiency, sophisticated architectures such as the Carry Select Adder (CSA) or Carry Look-Ahead Adder (CLA) can be investigated. The study thus establishes a basis for scaling the designs to larger bit-widths and more efficient adder architectures for future low-power VLSI applications, in addition to proving the superiority of the 10T SERF technique in existing implementations.

5. REFERENCES

[1] Chandran venkatesan and Thabsera sulthan ,"Analysis of 1 Bit full Adder using different Techniques", in International Conference on advanced computing and communication systems (ICACCS), 2019,IEEE.

[2] Nidhi Kedia and Kunal, "GDI Technique : A power efficient technique for Digital Circuits," in ISSN (Print) : 278 -8948 ,vol.1,2012,pp.87–93.

[3] Srikant M Patar and Ravish Aradhya H V, "Novel low power and High speed 8T full adder," in International Journal of Scientific and Engineering Research, vol.4, Aug. 2016, pp. 1156–1160.

[4] Mr. Bavusaheb Kunchanur and Mrs. Swapna Srinivasan, "Design and analysis of full adder using different Low power Techniques," pp.1-4.

[5] Chandran V, Elakkiya B, "Energy Efficient and High-Speed Approximate Multiplier Using Rounding Technique", Journal of VLSI Design and Signal Processing 3(2,3)

[6] Manjunath K M, Abdul Lateef Haroon P S, Amarappa Pagi, Ulaganathan J, "Analysis of various full-adder circuits in Cadence in,"International conferences on Emerging Research" in Electronics Computer Science and Technology,2015, pp. 90–97.

[7] Ms. Asha K A and Mr. Kunjan, Shinde D, "Analysis, Design and Implementation of full adder for systolic array based architectures," in IOSR Journal of VLSI and Signal Processing, vol.6, May-Jun. 2016 ,pp. 73–77.

[8] Chandran V, Ali K S, Gnanaprakash V, "Energy Efficient and HighSpeed Rounding-Based Approximate Multiplier".

[9] Rohit Kumar and Sachin Tyagi,"Design of low power full adder in 0.18um CMOS technology," in International Journal of Engineering Sciences and Research Technology , Aug.2016, pp. 446–456.