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A Power-Efficient 32-Bit ALU Using 16 Nm Finfet Technology Based NCL Standard Cells For Asynchronous VLSI Systems

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Abstract *– The need for low-power, high-speed computing in nanometer-scale technology nodes has driven innovation in asynchronous design paradigms. Null Convention Logic (NCL), a delay-insensitive asynchronous methodology, eliminates the global clock and enhances power efficiency. In this paper, we propose a novel 32-bit Arithmetic Logic Unit (ALU) designed using NCL standard cells implemented with 16nm FinFET technology. A complete library of 27 NCL threshold gates was developed and characterized using Cadence tools and the Synopsys ecosystem. The FinFET-based NCL gates show significant improvements in delay (up to 16.5%) and power (up to 7.2%) over static and semi-static CMOS equivalents. The ALU design leverages the robustness and energy benefits of NCL and FinFETs, and is validated through full custom layout, simulation, and performance benchmarking. The proposed design demonstrates promise for asynchronous embedded and low-power VLSI systems.*

Keywords– *Null Convention Logic (NCL), Asynchronous Design, FinFET, Threshold Logic Gates, Power-Delay Product, Standard Cell Library, ALU, Dual-Rail Logic, Completion Detection*

INTRODUCTION

VLSI systems today encounter increasing challenges due to clock distribution complexity, power density, and variability, especially as technology scales below 22 nm. Synchronous design, despite being the dominant digital logic style, faces limitations such as clock skew, jitter, and power inefficiencies. Asynchronous design paradigms, particularly Null Convention Logic (NCL), offer potential advantages in the design of energy-efficient and resilient systems.

NCL is a quasi-delay-insensitive (QDI) asynchronous logic style which eliminates the need for a global clock and uses dual-rail encoding and handshaking protocols for communication [1]. On the device front, FinFETs provide superior electrostatic control, reduced leakage, and improved drive strength compared to planar MOSFETs, making them ideal for modern low-power circuit implementations.

This paper details the implementation of a 32-bit ALU using a newly developed library of NCL standard cells realized with 16nm FinFET devices. The work includes threshold gate architecture optimization, cell-level characterization, and complete design and evaluation of an ALU architecture.

NULL CONVENTION LOGIC PARADIGM

Null Convention Logic is a novel technique for building an asynchronous designs. NCL is a delay-insensitive circuit technique, which is type of a DI (delay-insensitive) called Quasi Delay- Insensitive design paradigm. The technique employs symbolic completeness and completeness of inputs to achieve delay-insensitive behaviour. NULL is used in NCL when there is no data or spacer between two related data [2]. NULL denotes the absence of any input or output. Isochronic Forks are used to create QDI, with similar fan-out delay. Null Convention Logic (NCL) enables digital logic to function without the need for a clock signal. It uses dual-rail data encoding to indicate valid and NULL states for each bit, with each logic function implemented through threshold gates with hysteresis properties [3].

A. Dual-Rail Encoding

Each binary signal is represented by two wires (D1, D0):

- Logic 1 → D1=1, D0=0
- Logic 0 → D1=0, D0=1
- NULL → D1=0, D0=0

B. Threshold Gates

Discrete threshold gates are utilized in the implementation of NCL designs. The logic symbol of a threshold gate with n number of inputs and m threshold value, known as THmn, is shown in Figure 1. The gate outputs the DATA when the input has the required threshold number of signals or wires [4].

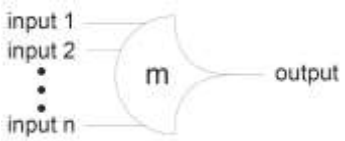


Fig. 1. THmn Threshold Gate

THmn w1w2...wR is another sort of threshold gate that utilizes integer weights as shown in Figure 2.

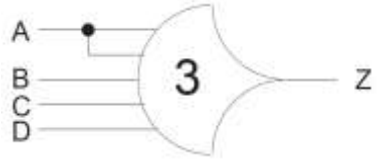


Fig. 2. TH34w2 Weighted Threshold Gate

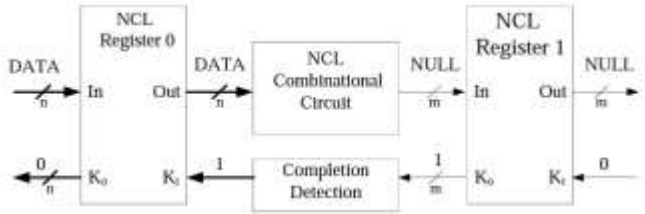
NCL-based circuits are mainly comprised of 27 principal threshold gates, as appeared in Table I. This gates make all possible sets of logic function comprising of maximum 4 variables. Each wire (rail) of an NCL flag is considered a distinct variable. 4 variables don't work the same as that of 4 literals, as 4 variables in NCL dual-rail implementation comprise 8 signals (e.g., a literal consists of both a variable and its counterpart(complement) [5].

TABLE I. THE FUNDAMENTAL NCL GATES.

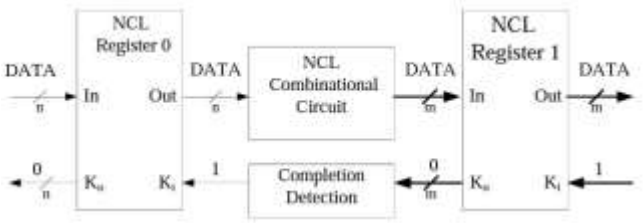
Sr. No.	NCL Gate	Logic Function
1	TH12	X + Y
2	TH22	XY
3	TH13	X + Y + Z
4	TH23	XY + YZ + ZX
5	TH33	XYZ
6	TH23w2	X + YZ
7	TH33w2	XY + XZ
8	TH14	X + Y + Z + W
9	TH24	XY + XZ + XW + YZ + YW + ZW
10	TH34	XYZ + XYW + XZW + YZW
11	TH44	XYZW
12	TH24w2	X + YZ + YW + ZW
13	TH34w2	XY + XZ + XW + YZW
14	TH44w2	XYZ + XYW + XZW
15	TH34w3	X + YZW
16	TH44w3	XY + XZ + XW
17	TH24w22	X + Y + ZW
18	TH34w22	XY + XZ + XW + YZ + YW
19	TH44w22	XY + XZW + YZW
20	TH54w22	XYZ + XYW
21	TH34w32	X + YZ + YW
22	TH54w32	XY + XZW
23	TH44w322	XY + XZ + XW + YZ
24	TH54w322	XY + XZ + YZW
25	THXOR0	XY + ZW
26	THAND0	XY + YZ + XW
27	TH24COMP	XZ + YZ + XW + YW

C. Completion Detection

Completion logic verifies whether all inputs have transitioned to either DATA or NULL states, facilitating safe and robust handshake signaling as shown in Figure 4. The hysteresis and delay-insensitive features of NCL make it highly suitable for low-power, high-noise-immune systems.



(a)



(b)

Fig. 3. Data Computation (a) Data Wavefront (b) Data Completion Detection

Figure 5 shows N bit Completion detection Tree structure for Feedback path [11].

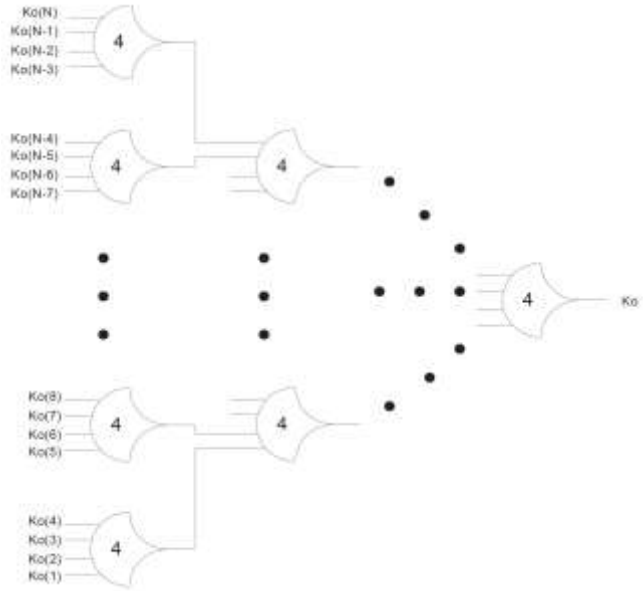


Fig. 4. N-bit Completion Detection Component

II. Design and Characterization of NCL Threshold Cells

A. Static and Semi-static Implementations

Initial threshold gate designs used static CMOS and semi-static variants. These structures rely on feedback loops and precharge mechanisms to hold state and transition between logic levels [6].

B. FinFET Device

FinFET devices are non-planar, multi-gate transistors fabricated on a silicon-on-insulator (SOI) substrate. As depicted in Figure 6, unlike planar MOSFETs, FinFETs feature a "fin" structure that extends over the channel region between the source and drain terminals. The lateral thickness of the fin determines the device's channel length [7].

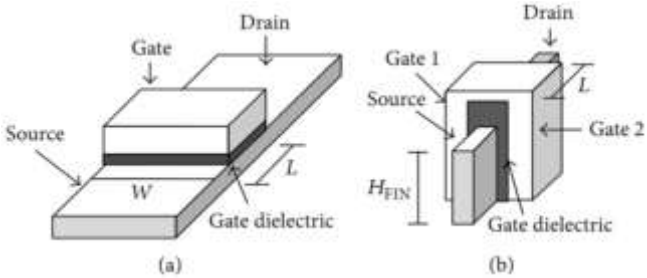


Fig. 5. Structural difference (a) Planar MOSFET (b) Multi-gate Fin-FET

Dual-gate FinFETs (DG) can be further classified as Shorted-Gate FinFETs and Independent Gate FinFETs. As shown in Figure 7(a), shorting both the front and back gates enhances the drive strength and channel control. However, this configuration results in higher power consumption. On the other hand, IGFinFETs are formed by growing an epitaxial oxide layer on top of the fin, isolating the vertical gates, as illustrated in Figure 7(b). This arrangement allows both gates to operate independently, leading to an overall reduction in circuit area [8]. A single IG-FinFET can function as two parallel MOSFETs. IG-FinFETs offer improved timing performance by reducing parasitic effects.

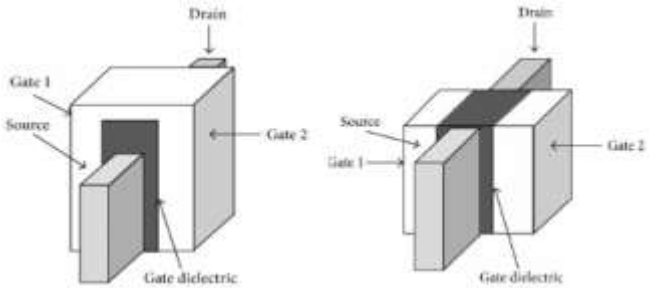


Fig. 6. FinFETs (a) Shorted Gate (SG) (b) Independent Gate (IG)

C. Proposed FinFET-Based Architecture

The newly proposed design utilizes FinFETs to construct state-holding feedback loops more efficiently as shown in Figure 8. The architecture reduces power leakage, improves switching behavior, and reduces area.

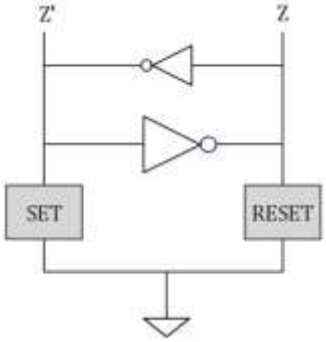


Fig. 7. Proposed structure for NCL gate implementation with SG-FinFET

D. Library Development and Tool-chain

The library of 27 threshold gates was designed using the ASAP7 PDK (7nm) and 16nm Predictive Technology Models (PTM). Following tools from cadence are used for implementing and characterizing the 27 fundamental NCL gates cell library:

- Virtuoso : Transistor Level Schematic design
- Spectre ADE : To simulate the design
- Layout XL : To prepare layout of the Design
- Virtuoso : To extract GDS
- Liberate : For Characterizing the NCL Cells
- Ocean Scripting: Automated variation analysis

TABLE II. PERFORMANCE COMPARISON BETWEEN DIFFERENT NCL GATE IMPLEMENTATIONS WITH CMOS AND FINFET DEVICES.

Device	NCL Gate	TpHL (pS)			TpLH (pS)			Avg. Power (uW)			No. of Transistor		
		Static	Semi-static	Proposed	Static	Semi-static	Proposed	Static	Semi-static	Proposed	Static	Semi-static	Proposed
CMOS	TH22	91.49	278.80	241.90	135.50	104.20	141.28	0.78	1.92	0.65	12	8	8
	TH23	97.27	228.70	221.70	130.20	66.71	97.85	0.78	1.70	0.67	20	12	12
	TH33	98.29	39.48	41.23	138.80	48.75	79.52	0.41	1.14	0.34	16	10	10
	TH24COMP	70.28	135.80	91.45	105.42	100.53	70.97	1.52	2.28	1.38	18	12	12
	TH34W2	81.18	142.96	83.52	121.77	105.31	65.68	1.61	2.42	1.56	22	15	15
SG-FinFET	TH22	27.14	50.94	37.80	27.46	28.22	36.56	0.59	1.02	0.51	12	8	8
	TH23	30.69	77.41	47.54	28.86	29.91	27.89	0.64	1.18	0.63	20	12	12
	TH33	33.99	76.05	61.25	33.45	34.71	31.56	0.32	0.58	0.35	16	10	10
	TH24COMP	21.52	101.54	57.52	48.59	89.56	71.45	0.52	0.78	0.49	18	12	12
	TH34W2	23.58	112.25	60.14	51.24	96.57	58.59	0.61	0.92	0.54	22	15	15

E. Power and Timing Analysis

The simulation results in Table II show that proposed NCL gate structure exhibits average 16.5% improvement in speed compare to its semi-static variant and average 7.2% reduction in power dissipation compare to its static variant. The proposed structure is on average 35% area efficient (in terms of number of transistors) compared to static NCL implementation. Semi-static structure has same number of transistors as in proposed structure due to its conceptual similarity with respect to functionality. Also, compare to static designs, semi-static designs consume approximately 17%

more average power for CMOS and FinFET devices. This is due to excess power required in inverter loop. In terms of average propagation delay per operation, Semi-static designs are 18.3% slower compare to its static counterpart. Number of transistors are less in semi-static designs due to removal of HOLD0 and HOLD1 block. Overall improvement on area utilization strongly depends of transistor sizes in inverter loop [9].

TABLE III. PDP AND AREA COMPARISON BETWEEN DIFFERENT NCL GATE IMPLEMENTATIONS WITH CMOS AND FINFET DEVICES

Device	NCL Gate	Power-Delay Product			No. of Transistor		
		Static	Semi-static	Proposed	Static	Semi-static	Proposed
CMOS	TH22	88.13	366.72	88.00	12	8	8
	TH24w2	70.51	132.60	59.80	20	14	14
	TH33	49.04	164.29	30.37	16	10	10
	TH23	89.21	251.39	80.94	20	12	12
SG-FinFET	TH22	31.44	55.65	27.44	12	8	8
	TH24w2	28.65	74.10	22.74	20	14	14
	TH33	26.15	47.48	26.00	16	10	10
	TH23	34.22	78.57	29.94	20	12	12
IG-FinFET	TH22	18.54	34.56	15.12	10	8	8
	TH24w2	14.65	39.78	13.80	18	12	12
	TH33	16.56	30.21	15.24	14	10	10
	TH23	18.90	35.01	12.59	16	10	10

The power-Delay Product for CMOS and FinFET based implementation is compared for different threshold gates as per Table III. The proposed structure exhibits average 14.56% reduction in PDP compared to static variant and average 61.87% reduction in PDP compared to its semi-static variant across different devices. Gate structure with IG-FinFET required less number of transistors because two parallel connected MOSFETs can be replaced with one IG-FinFET.

III. 32-BIT ALU DESIGN USING FINFET NCL CELLS

A. ALU Architecture Overview

32-bit ALU is a fundamental computing block used in microprocessors and DSPs. It performs arithmetic and logic operations such as addition, subtraction, AND, OR, XOR, and shift operations. The NCL-based ALU is implemented using dual-rail logic, threshold gates, and completion detection circuits to ensure proper handshaking between pipeline stages [10].

The ALU supports a set of core operations:

- Arithmetic: Addition, Subtraction
- Logical: AND, OR, XOR
- Shift: Logical left/right, Arithmetic right

The ALU architecture consists of:

- A 32-bit ripple-carry adder/subtractor implemented with TH22-based full adders [12]
- Bitwise logic unit using TH13 and TH33 gates
- 32-bit barrel shifter implemented using a hierarchical shift structure
- Dual-rail operation select logic with completion detection

Figure 9 shows the high-level block diagram of the ALU.

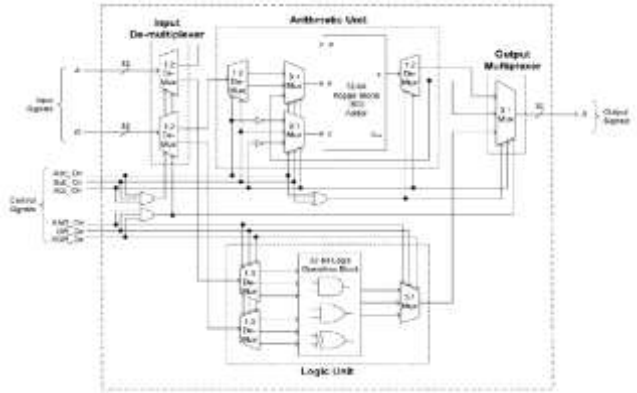


Fig. 8. Block diagram of the 32-bit ALU with dual-rail data path and control logic.

B. Design Flow

- RTL functional model written in Verilog
- Synthesis using Cadence Genus

- Floorplanning, placement, and routing in Innovus
- Post-layout simulation using Spectre

C. Performance Analysis

Post-layout simulations were conducted for both FinFET-based and traditional CMOS-based NCL implementations of the 32-bit ALU. Table IV indicates the comparison of both implementations for various performance criteria.
It is observed here that

- Speed: FinFET's lower capacitance and higher drive strength significantly reduced delay.
- Power: Sleep-enabled NCL circuits and efficient FinFET leakage control leads to energy and power savings.
- Area: There will be no much change in transistor counts, as the SG-FinFET and CMOS device occupies a similar area with nearly equal transistor count.

TABLE IV. COMPARATIVE METRICS

Performance Metric	FinFET NCL (16 nm)	CMOS QDI (65 nm)	Improvement (%)
Propagation Delay	~80.5 ns	~120.5 ns	32%
Energy per Operation	~11 pJ	~18 pJ	39%
Idle (Leakage) Power	~90 nW	~160 nW	0.44

The design, implementation and validation of the 32-bit NCL-based ALU using 16nm FinFET technology confirm the scalability, performance, and efficiency of the proposed standard cell library.

CONCLUSION AND FUTURE SCOPE

Through various studies and analysis it is concluded that, Asynchronous VLSI designs offer several advantages and unique features compared to their synchronous counterparts. By eliminating the need for a global clock signal, asynchronous designs can provide improved power efficiency, reduced circuit complexity, and increased robustness against variations in process, voltage, and temperature.
However, designing and verifying asynchronous circuits can be more challenging due to the lack of a global clock reference. Asynchronous designs require careful consideration of timing hazards, metastability issues, and the potential for data races. Specialized design methodologies, such as delay-insensitive and NULL convention logic (NCL), have been developed to address these challenges and ensure correct operation at lower technology node.
The proposed NCL gate structure exhibits average 16.5% improvement in speed compare to its semi-static variant and average 7.2% reduction in power dissipation compare to its static variant. The proposed structure is on average 35% area efficient (in terms of number of transistors) compared to static NCL implementation.
NCL has found applications in various domains, including communication systems, signal processing, and control circuits. Its robustness and low-power characteristics make it particularly suitable for battery-powered devices, wearable electronics, and other energy-constrained applications.
The scope of NCL lies in its applicability to asynchronous systems, making it a viable option for designs that do not rely on a global clock signal. Its delay insensitive nature allows for robust operation in the face of timing variations, making it suitable for applications where process, voltage, and temperature variations are a concern. NCL finds particular value in low-power applications, where its inherent power efficiency can be advantageous.
However, NCL also has its limitations. The design complexity of NCL circuits should not be underestimated, requiring careful consideration of encoding schemes, handshaking protocols, and synchronization between components.

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