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"Dynamic Voltage Scaling For Low-Power VLSI Design: A Review Of Power Optimization Techniques And Memory Efficiency Enhancements"

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Abstract *– The increasing demand for energy efficient devices, from mobiles systems to high performance computing, has made VLSI design a crucial study topic. Battery life, heat dissipation, and overall system reliability are all directly impacted by power usage. Dynamic Voltage Scaling (DVS), one of the best power management strategies, dynamically modifies the supply voltage and significantly lower power usage without noticeably compromising performance in response to workload demands. By altering the operating voltage of a processor or circuit block in reaction to variations in workload. DVS aids in the optimization of both dynamic and leaky power. The system runs at a lower voltage while processing demands are minimal, but large computational loads cause the voltage to rise in order to sustain performance. This study reveals the various power management techniques and compares the performance to give suitable method for particular application. By decreasing voltage levels during idle times, DVS lowers standby power consumption in memory units and increase memory efficiency.*

Keywords *– 1. Dynamic Voltage scaling 2. Power Gating 3.Clock Gating 4. Low Power Design 5. Power Management Techniques.*

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1. INTRODUCTION

Transistor density has increased due to the quick development of semiconductor technology, which has raised questions about heat production and power dissipation. Conventional Techniques for Power Reduction are Optimizing transistor size to save power consumption is known as transistor sizing. To conserve dynamic power, clock gating involves turning off the clock signal to track blocks not being used. Power gating reduces leakage power by shutting off entire circuit blocks when not in use[5].

High-threshold transistors are used in multi-threshold CMOS (MTCMOS)[8] to reduce leakage in standby mode. Operand Isolation technique isolates the circuit's inactive components to save needless switching. Techniques for bus encoding are lowering data bus switching activity to cut down on power consumption. Drawbacks of these methods are Decreased Scalability: Static methods might not be able to adjust to changing demands. Enhanced Design Complexity: More control systems and circuitry are needed.Problems with Latency: Certain methods cause delays while switching between power states. Limited Leakage Power Reduction: In deep-submicron technology, leakage power is a problem for conventional techniques. Performance trade- offs: Performance may suffer from aggressive power reduction. Area Overhead: Techniques like clock gating and power gating require more transistors and logic. By dynamically modifying the supply voltage in response to workload demands, DVS significantly reduces dynamic and leakage power. Research and development in low-power Very Large Scale Integration (VLSI) design has become crucial due to the increasing need for high-performance, energy-efficient electronic products. Optimized power consumption is necessary for modern electronic systems, such as mobile devices, embedded systems, and high- performance computing, in order to prolong battery life, lower heat dissipation, and increase overall system reliability. DVS is one of the best methods for lowering power consumption in VLSI circuits. A power management method called DVS dynamically modifies the supply voltage in response to processing demands in real time. Reducing voltage is considerably lower power consumption while preserving the required performance levels because power consumption is proportionate to the supplied voltage squared. The article is organized as section2 discuss various research in the proposed method. Section 3 is described about DVS with relevant techniques. Section 4 gives the comparison all methods.Section5 conclude the work.

2. BACKGROUND:

Michael Keating et.al,2007,'[1]', In cooperation with dynamic and static power makes up a SoC design's overall power. Dynamic power is the amount of power used while the gadget is in operation. Static power is the amount of power utilized while the device is stationary. Static power consumption in CMOS devices is caused by leakage. Dynamic power utilization is typically caused by switching power, which is the power necessary to charge and discharge a gate's output capacitance. Many architectural, logic, and circuit design techniques can be used to diminish the power for a convinced task implemented in a known technology. These methods concentrate on the voltage and frequency method of the equation while lowering the data-dependent switching activity. Numerous architectural and logic design strategies are available to reduce switching activity, which in turn reduces switching activity for the relevant gates. Because power and voltage have a quadratic relationship,lowering the supply voltage is a highly effective strategy for lowering dynamic power. However, as supply voltage drops, a gate's speed also drops. SoC designers can benefit from this strategy in a number of ways:

- For peripherals and other blocks that don't need to run very fast, it can utilize a lesser voltage supply than other, extra speed-critical blocks. This technique is known as multi-voltage.

* It can offer processors with a changeable supply voltage; for applications that demand optimal routine, it can give both a high supply voltage and a elevated clock frequency. For less routine tasks, it can offer a slower clock and lower voltage. This technique is known as voltage scaling.

Clock gating is a further method for reducing dynamic power. The power drops to zero when the frequency drops to zero. Many SoC architectures use clock gating in one way or another.

The most excellent method to diminish dynamic power is to lesser the supply voltage. More than fifteen years, VDD has dropped from 5V to 3.3V to 2.5V to 1.2V as semiconductor technology has improved. The ITRS road map states that in 2008 and 2009, elevated routine devices will use 1.0V and low power devices will employ 0.8V. Lowering VDD has the drawback of often lowering IDS, the transistor's on or drive current, which causes slower speeds. The IDS for a MOSFET can be roughly calculated by ignoring velocity saturation and a few other minor effects that happen below 90 nm.

$IDS = \mu C_{OX}\ W/L(VGS\text{-}VT)^2$

$IDS = \mu C_{OX}\ W/2L.(VGS\text{-}VT)^2$ [1]

Where the gate capacitance is Cox, the threshold voltage is VT, the gate-source voltage is VGS, and the carrier mobility is μ. The four chief issues of leakage currents in CMOS gates are reverse bias junction leakage (IREV), gate leakage (IGATE), gate induced drain leakage (IGIDL), and sub-threshold leakage (ISUB).The most straightforward application of this innovative technique is to divide the inside circuitry of the chip into numerous voltage regions, each with its personal supply. Multi-voltage design is the term for this method. It is based on the knowledge that different blocks in a recent SoC design have different routine objectives and constraints.

Assigning dissimilar blocks, steady supply voltages is known as static voltage scaling, or SVS.

An expansion of MVS, DVFS involves dynamically switching a greater number of voltage levels in response to changing workloads.

- Adaptive Voltage Scaling (AVS): DVFS expanded to include a control loop for voltage adjustment.

including power gating; and explicitly hold power gating by Michael Keating et al. (2007), "[1]," any of the following techniques may be used when the IP is actually implemented on a chip: multi VT, voltage scaling, clock gating, and power gating.Wenxin Wang et.al,2007,[2],The primary function of portable devices is power indulgence. Various power indulgence are shown in Figure 1.

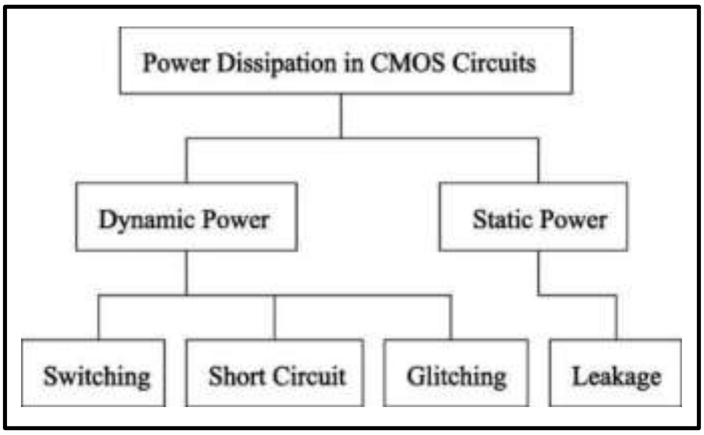


Figure 1. Various Power Indulgence in CMOS circuits

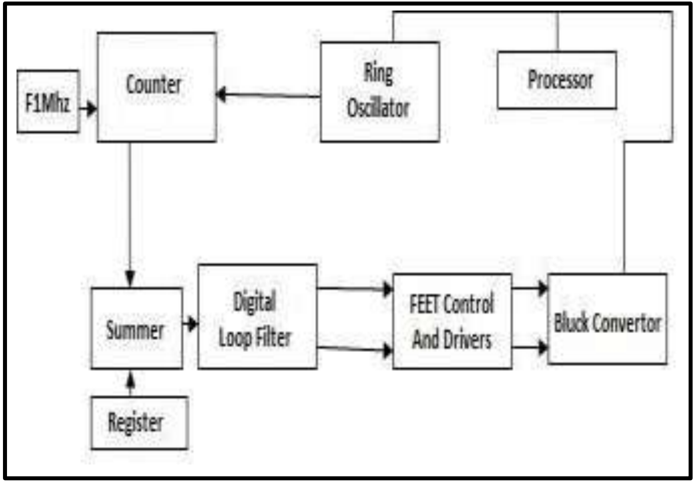


Figure 2. Dynamic Power

$P_{avg} = P_{dynamic} + P_{shortciaui} + P_{leakage} + P_{static}$ [2]

Dynamic power is defined as Energy/ transition = CL*Vdd^2

1) Circuit capacitance charging and discharging is the cause of dynamic power dissipation.

It must build an IP to work with various power strategies in order to ensure that it can be used efficiently in a variety of low-power applications. Clock gating with several VT $P_{dynamic} \square CL * V_{dd}{}^{2} * N * f$ [3]

libraries may be able to supply little adequate power in one application. In additional applications, destructive on-chip power gating can be necessary. In a few applications, dynamic voltage scaling may be the answer to achieving the chip's power requirements. To tackle a lot of requests, it should do the follow: Plan the clocking and retune approach Vdd is the supply voltage, f is the operating frequency, N is the switching motion, and CL is the output load capacitance.

2) The signal's rise and fall timings are the cause of short circuit power dissipation.

with low power in intellect; package the intellectual property to enable low power; create reference power intent files; divide the design to accept multiple less power techniques, n $P_{shortcircuit} \square K(V_{dd} \square 2V_{th})^{3} * \square * N * f$

[4]

K is the transistor's size, N is the average number of transitions, f is the clock frequency, and τ is the input signal's rise and fall time.

3) Sub threshold conditions and reverse bias leakage current are the causes of leakage power dissipation.

$I_{leakage} \square I_S (\exp(V_{dd} / V_T \square 1))$ - [5]

D.KoteswaraRao, 2014, "[3]", Sequential circuits achieve a fine-grained integration of CG and RTPG. First, a fine-grained, activity-driven OBSC method that only chooses a portion of FFs to gate is assessed. Additionally, the sleep signal in RTPG can be the clock enable signal produced in the OBSC circuit. Subsequently, Tanner Tools is used to assess the performance of sequential circuits that incorporate both OBSC and RTPG utilizing the sleep and variable body bias techniques.

Because of a path that exists between the power source and ground due to PMOS transistors in the circuit described [4], The power consumed by the circuit when it is not in use is known as static power dissipation. This can be decreased using a variety of strategies that were previously suggested in low power design methodologies. Various circuit strategies are employed to provide the best performance while keeping power consumption (both static and dynamic) within a certain range [5].Techniques for Dynamic Voltage Scaling (DVS) have been thoroughly researched in order to improve VLSI circuit power efficiency. A workload-aware DVS method that dynamically modifies voltage levels in response to real-time processing demand was proposed [6]. Adaptive voltage scaling (AVS), first presented [7], makes use of feedback loops to optimize power usage in response to changes in process and temperature. Multi-level DVS showed how effective it is at managing variable workloads with little latency overhead [8]. By way of the superior expertise of VLSI circuit designs, energy competence can be obtained through the use of the DVS system. It examines the research on energy-efficient development in real-time systems on DVS platforms to address both notional and realistic issues [9]. Many studies have looked into DVS as a useful method for reducing power consumption in VLSI circuits.. Numerous studies have investigated various approaches to optimize DVS for low-power applications in high-performance CPUs, embedded systems, and mobile computing.

DVS, is the suggested method for lowering microprocessor power and energy usage. Lowering the working frequency fclk alone can lesser power utilization without altering energy use because the computation takes longer to end. Reducing the supply voltage Vdd can save a major source of energy since quadratic relationship between power and Vdd, which is given by Equation 2. Diminishing the supply voltage and working frequency scale can further cut down on power and energy usage. Incorporate the dynamic voltage scaling technique into the scaling scheme of the real-time operating system. This calculates how much work will be done in the next time slot and then modifies the clock frequency and supply voltage to enhance system performance [10-11].When the schedule with the lowest constant speed can be outperformed using with two different speeds. Furthermore, the constant speed schedule remains the best option for reducing the crest heat while scheduling a recurring job set while the temperature is at its steady state [12,13]. Clock gating is a hardware method that reduces dynamic power utilization by cutting off the clock signal to components that are not employed. The clock signal is halted to avoid needless switching activity while a CPU module is not in use. It is used in Microcontrollers, FPGAs, and mobile processors. This method is reduces superfluous switching power and easy to incorporate into hardware design. Some limitations are leakage power cannot be reduced and not is use, if the majority of the system's components are running. Instead of just stopping the clock signal, power gating stops the power supply to circuits that are not in use. Leakage power is a major problem with deep submicron CMOS technology, but this technique significantly reduces it.

It uses transistor-based power switches to fully turn off inactive parts. In multi-core computers, this is frequently achieved by turning off dormant cores and minimizes idle circuit power leakage. It increases the low-power VLSI design's energy efficiency and regulating power usage when turning parts on and off and may cause lags in performance. Multiple Voltage Domains allow for autonomous power control by using different voltage levels for various system components. Energy-efficient cores operate at lower voltages, whereas high-performance cores operate at higher voltages and utilized in ARM large and other heterogeneous computing systems. It minimizes needless power usage in low-priority processes and optimizes power and performance for various workloads. Energy-aware scheduling minimizes power usage by allocating jobs to CPU cores. Real-time embedded systems and operating systems both make extensive use of this technology. Scheduling algorithms lower the number of active cores to conserve power, and workload balancing effectively divides activities to avoid overheating. Multiple sleep phases are supported by contemporary CPUs and embedded systems, which lowers power consumption during system idle. High power usage raises the temperature, which might shorten the lifespan and dependability of the system. In order to avoid overheating, thermally aware power management strategies keep an eye on temperature sensors and dynamically modify power settings. Because power α V2, lowering the supply voltage quadratically reduces power usage. Frequency scaling: Dynamic power consumption decreases linearly (power α f) when the clock frequency is lowered. Combined Scaling: By modifying both variables, low energy consumption is guaranteed without sacrificing performance. In an attempt to combine the best aspects of the two earlier concepts, a hybrid of both was developed. Restrictive the dynamic voltages to a tiny division of just a minimum values can greatly simplify the power supply circuit even if each core must have access to changeable voltages [14]. Voltage regulators produce these voltages either on-chip to lower package pin counts or off-chip to lower cooling system pressures. This method provides the greatest versatility because it can handle a wide range of voltage domains and be readily scaled up or down to accommodate processors with various architectures. As a 167-core processor platform, is one of numerous many-core chip designs that use this strategy [15] [16].

M. Uma Maheswari, 2014."[17]", A new circuit topology called a "dual stack" that offers designers a solution for both static and dynamic power. The dual stack strategy preserves the initial state, in contrast to the sleep transistor technique. Out of all the approaches, the twin stack approach exhibits the lowest speed power product. Consequently, designers that need ultra-low leakage power consumption with significantly lower speed power product have new options thanks to the dual stack approach. In particular, it displays between 50 and 80 percent more power than the current standard or conventional full adders. Thus, it can be applied to integrated circuits in the future for area and power efficiency.

Bojan Jovanović* and Milun Jevtić ,2012, "[18]",We outline a few popular methods for minimizing both static and dynamic power in contemporary VLSI designs. These methods can be used at several phases of the system design, from the top level, which handles the architectural changes of the design, down the technology level, where the designer can alter technology parameters (transistor sizes, supply, and threshold voltages).

3. LOW POWER TECHNIQUES AND VOLTAGE SCALING TECHNIQUES

All design abstraction levels must be optimized for an integrated low power technique, as given below:

1. System: Power reduction and partitioning.
2. Algorithm: Design complexity, operation concurrency, and consistency in operation.
3. Architecture: Data encoding and decoding, process pipelining, data redundancy, and parallelism.
4. Circuit Logic: Component sizing, energy recovery techniques, and logic design styles.
5. Technology: Multi-Threshold Devices, Threshold Reduction Capability.

By adjusting the single voltage to the routine command, dynamic supply scaling eliminates the need for two power sources (static supply scaling). By the highest intended frequency of process, the best routine is achieved with the highest supply voltage. Lowering the supply voltage and clock frequency only provides the necessary routine with a significant power reduction when routine command is low. Adaptive Voltage Scaling (AVS) uses a closed loop technique to produce the buck operating voltage for an explicit processing frequency [13]. The AVS loop regulates processor routine by routinely adjusting the power supply's output voltage to take into consideration changes in the CPU's temperature and operation [14]. Power supply tolerance is also eliminated by the AVS loop and compared to open-loop voltage scaling methods similar to DVS, AVS uses up to 45% lower energy.

4. SCALING OF DYNAMIC VOLTAGE

Burd and Robert Thomas D. (2000), "[13],"In portable electronics, time-varying performance needs are usually part of the computational load on processors. A technique called dynamic voltage scaling modifies the processor's supply voltage to function at the lowest routine level required by the software processes that are currently performing while consuming the least amount of energy. Although the circuit design and design flow of a processor are affected by a dynamically changing supply voltage, it is simple to design a processor with this capacity given a few small restrictions. Figure 2 depicts the feedback loop that transforms a preferred in service frequency, FDES, into VDD. VDD is changed into a clock signal, fCLK, via the ring oscillator. fCLK is converted by a counter to FMEAS, a digital measured frequency value. The frequency error, or FERR, is *calculated by subtracting this value from FDES. The loop filter employs a mixture pulse-width/pulse- frequency modulation method to produce an MP or MN permit signal. The inductor L charges the capacitor C to make a VDD, which is subsequently fed reverse to the ring oscillator to end the round. In addition to the supply undulation and alteration efficiency routine dealings of a typical voltage regulator, the DVS converter introduces two additional performance metrics: transition time and transition energy.*

The transition time for a significant voltage shift (from VDD1 to VDD2) is:

$$t_{Trans} = 2C/I_{max}|VDD2-VDD1| \qquad [6]$$

where Imax is the converter's most output current and the triangular waveform of the current pulses results in a factor of 2. During this transition, the following energy is used:

$$E_{Trans} = (1-\eta).C\ |VDD2^{2} -VDD1^{2}| \qquad [7]$$

where η represents the DC-DC converter's efficiency.

By lowering supply wrinkle and raising low-voltage alteration effectiveness, raising C improves the loop's voltage regulation capabilities while declining C makes it a better voltage tracking system. Thus, in order to reduce C and minimize energy and transition time, the main trade-off in the design of a DVS system is to enhance the processor's tolerance to supply ripple.

The best power management technique for energy- efficient computing is still DVS. Three essential elements are needed to apply the DVS approach in processors:

1. An operating system that cleverly adjusts the speed of the CPU. 2. A control loop that produces the requisite voltage at the necessary speed. 3. A microchip that can function throughout a voltage variety.

Two separate tasks form the basis of the DVS algorithm:

(i) the frequency setting policy, which maintains constant performance by adjusting the CPU frequency and voltage based on the current entrance and decoding tariff, and (ii) the change point detection algorithm, which recognizes variations in arrival or decoding rates. [19]. On hard real- time systems, the dynamic-mode DVS algorithm saves 15% on average more energy than the conventional two-mode DVS method. A preliminary test of our suggested technique is also implemented, and energy changeover overhead is taken into account[20]. It outlined the compositional scheduling framework's real-time DVS problem. In view of the intermittent resource model, it provide the most favorable static DVS methods at the task, component, and system levels. In order to achieve even greater energy savings, Additionally, it presents DVS systems at the module and mission levels that exploit resource availability and runtime underutilized slack moments[21]. Finally, it provides algorithms for monotonic scheduling and power-aware scheduling requirements to guarantee that all DVS components are viable for the Rate and the Earliest Deadline First. Classification of DVS Power Management Techniques is shown in Figure 3.

The OS's task administration service and real-time scheduler are customized by narrative algorithms called real- time DVS (RT-DVS) to offer noteworthy energy reserves while maintaining real-time target guarantees. These RT- DVS algorithms directly be similar to the hypothetical lesser bounce on energy utilization, and illustrate from side to side simulations and a working prototype realization that they can easily diminish energy utilization in an embedded real-time system by 20% to 40% [22]. The main element of the DVS design is the dc-dc power control device, which is made especially to offer unpredictability on the Vdd. The implemented design can vigorously change the Vdd from 300 mV to 1.2V with an early setup time of 1.5 μsec. This research investigates the result of DVS on dynamic power indulgence in a Fast Fourier Transform multiplier core. When DVS is applied to the multiplier blocks, the average power reduction is 25%. 0.12μm ST was used to implement the design [23]. By altering the processor's operating voltage and frequency during runtime, DVS[24] have be demonstrated to capitalize on the significant fluctuation in processing requirements [25,26]. DVS is very useful for cutting down on idle time when workload is light. In an effort to save electricity, researchers have recently tried to use DVS for video decoding [27, 28].

It obtain experimental switching overhead data from a test device made on 90nm silicon. The overhead measurements demonstrate that fine-grained DVS can reduce energy usage by utilizing the transition to lower VDDs for as minimum as one arithmetic operation, and they also validate that the models we created provide acceptable estimation of the energy overhead [29]. By connecting the sensor placement process with the current thermal TSV planning step for 3-D ICs, we suggest a low-overhead design methodology. For the temperature sensor infrastructure, a portion of the thermal TSV resources are separated from their initial application. Trade-offs related to the decrease in thermal TSV resources are examined [30]

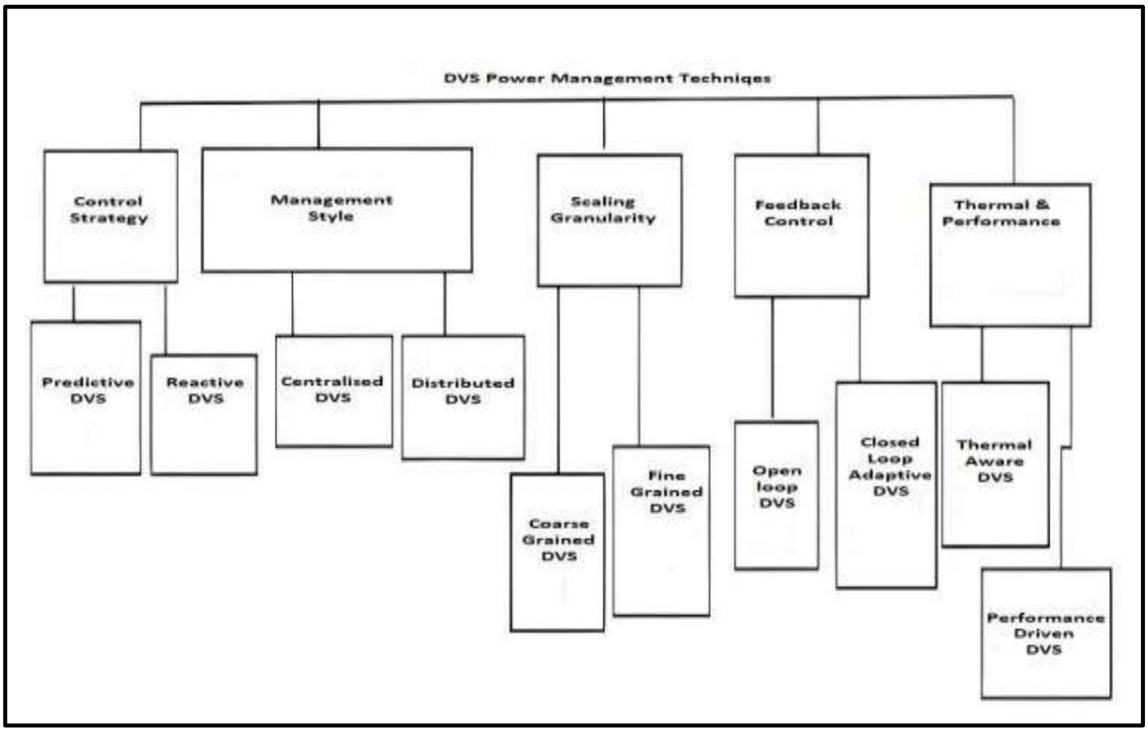


Figure 3. Classification of DVS Power Management Techniques

4.1 Summary of Recent Low Power Technique

Mohammad Sadrosadati et al ,2022,[31],Numerous methods are such as voltage scaling, power gating, and clock gating, demonstrating their effectiveness in reducing dynamic power. Additionally, advancements in low-power circuit design are studied, such as energy-efficient flip-flops and domino logic. System-level approaches use a variety of strategies, such as improving software algorithms and lowering component-to-component communication overhead, to maximize the system's overall power usage.

P. Srivastava et al ,2024,[32], Using AI and machine learning (ML) techniques in VLSI design and manufacturing reduces the time and effort needed to understand and process data inside and across different levels of abstraction. Consequently, it lowers the manufacturing turnaround time and increases the IC yield.

Deepthi Amuru et al ,2023,[33],The AI/ML automated techniques that were previously introduced for VLSI design and manufacture are reviewed. It uses diffusion models to show how closely synthetic data resembles real data. In the predictive analysis of VLSI design for digital circuits, we show that data augmentation is unquestionably useful and validate the quality of the created data.

Adwaitha S Pai et al,2024,[34], It examine several methods, including as voltage scaling, power gating, and clock gating, emphasizing their effectiveness in reducing dynamic power. Additionally, advancements in low-power circuit design are analyzed, such as energy-efficient flip- flops and domino logic. Through a variety of strategies, including software algorithm optimization and component- to-component communication overhead reduction, system- level approaches seek to maximize the system's overall power consumption.

Venkatesh Kodukula et al 2022,[35], According to our characterization, lowering the analog voltage applied to the image sensor improves sensor power efficiency but degrades imaging fidelity by making images noisier and brighter. Additionally, we discover that the task accuracy of vision applications is situational impacted by brighter and noisier images. In this poster, we suggest a study of a system that respects the fidelity requirements of visual activities while adaptively scaling analog voltage to maximize sensor energy.

Jason Manford et al ,2024,[36],In order to improve power efficiency in Field Programmable Gate Arrays (FPGAs), Dynamic Voltage Scaling (DVS) approaches are thoroughly examined in this work. It examines the body of research in the area, suggests an experimental approach to assess DVS efficacy, and talks about the difficulties and potential paths forward. The study comes to the conclusion that although DVS provides significant power savings, careful optimization is needed to balance performance trade- offs during installation.

Dostal, F. (2023), [37], Accurate Voltage Control with DVS: This method entails adjusting the output voltage to account for load fluctuations, guaranteeing accurate voltage control and improving system stability.
Chen, D 2024,[38], Island-Based Random DVS for Security: This novel technique improves security in cryptographic applications by introducing random voltage scaling over various areas (or "islands") of a semiconductor to counteract power side-channel assaults.
R. Kannan and R. Rangarajan 2020, “[39]” ,When compared to current noise-tolerant circuits, the suggested logic circuit has achieved a higher Power Delay Product (PDP). Comparing the suggested logic to the low power domino logic circuit for two input OR gates, the experimental simulation results demonstrate a 3.4% power saving. The latency in the current logics was somewhat compromised in the suggested logic. In contrast to current methods, the proposed logic circuit's Power Delay Product (PDP) has decreased. In comparison to the current logics, the suggested logic also offers a greater improvement in noise immunity metrics like UNG and ANTE. The suggested logic circuit-based application circuit, like the 4:1 multiplexer, also offers superior enhancement in terms of noise immunity and power consumption.

K. R. Haripriya et.al,2020, “[40]”, To increase power savings, a variety of low power strategies are used, such as power gating and multi-voltage. Verification of power awareness has thus become a crucial topic. To ensure that low power architectures are constructed correctly and adhere to all electrical regulations in SoC, static low power verification was created.All power purpose information is contained in the standardized UPF (Unified Power Format), which may be utilized to guarantee that the power specification is maintained throughout the design process.First, the particular cells and how they work in low power techniques are described in this paper. Second, it outlines the key tests that are done at every step using the Synopsys VCLP tool, followed by tool debugging and a conclusion.

Aoqi Yang 2025, “[41]”classification method of power optimization for digital integrated circuits as given:- By improving integration density, lowering voltage, and lowering I/O power consumption, low-power design at the process level optimizes energy efficiency in digital integrated circuits by efficiently using contemporary process and packaging technology. In addition to improving the circuit's overall performance, these actions offer solid support for the energy efficiency requirements of the upcoming generation of electronic gadgets.

Tan, S et.al,2020,“[42]”,Under a 0.7 V supply, a clockgating cell with a sleeping mechanism is suggested. Static power is reduced through the use of power gating. The suggested cell can normally be utilized in circuits with frequencies up to 1MHz. This study stands out from the current design due to its lower leakage current of 1.56 pA, which is appropriate for low frequency circuits that require a low power standard cell library.

In the traditional design, clock flipping accounts for at least 50% of the chip's dynamic energy consumption. With the use of clock gating technology, the chip's overall power consumption is significantly decreased when a portion of the system enters an idle state because the dynamic power consumption is eliminated, and the system's regular performance and operation remain unaffected.Weijun Hu ,2024, [43],Multiple blocks operating at the same supply voltage make create a power domain. Certain power domains function at voltage levels that are the same or different. For power management components, including level shifters utilized in the initial phases of VHDL modeling, the UPF offers constructs that are described. This enables designers to define the voltage levels of the blocks and group them into the power domain. The following are some of the strategies.
Clock transitions result in a considerable amount of power usage. The majority popular and extensively used low-power techniques are clock gating.

THREE LEVELS OF GRAININESS EXIST:

1. Module-level gating of clocks
2. Register-level gating of clocks

3. Clock gating at the cell level.

Cyclic power gating (CPG) minimizes disruption to running programs by enabling the core's power supply to be turned on or off while operating at high speed. By altering the duty cycle's on-off ratio during a single power-gating phase, the processor's effective frequency and power consumption are managed. To preserve the core's state during power gating, this approach requires a state-retentive architecture, despite being a great substitute for voltage frequency scaling (Kim et al., 2021).

Scaling of voltage

The supply voltage has a noteworthy shock on power utilization. Little power utilization can be achieved through supply voltage scaling. There are various kinds of voltage scaling, depending on how it is implemented.

- Scaling of static voltage (SVS)
- Voltage scaling at several levels (MVS)
- DVFS stands for dynamic voltage and frequency scaling.
- AVS, or adaptive voltage scaling
- Memory partitioning
- Bus Segmentation
- Hardware acceleration
- Reconfigurable hardware modules

The Figure 4 described the various optimization techniques of digital integrated circuits.

looked at application functions that use a lot of power in order to comprehend IoT applications. These functions are categorized as follows.

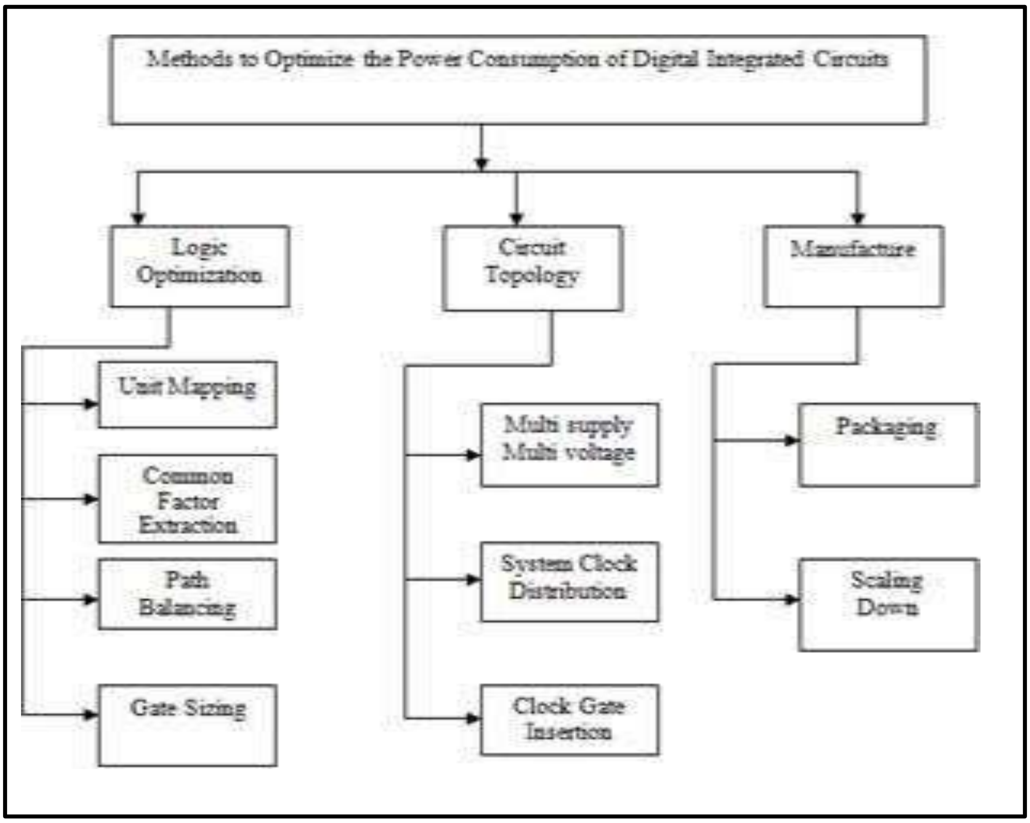
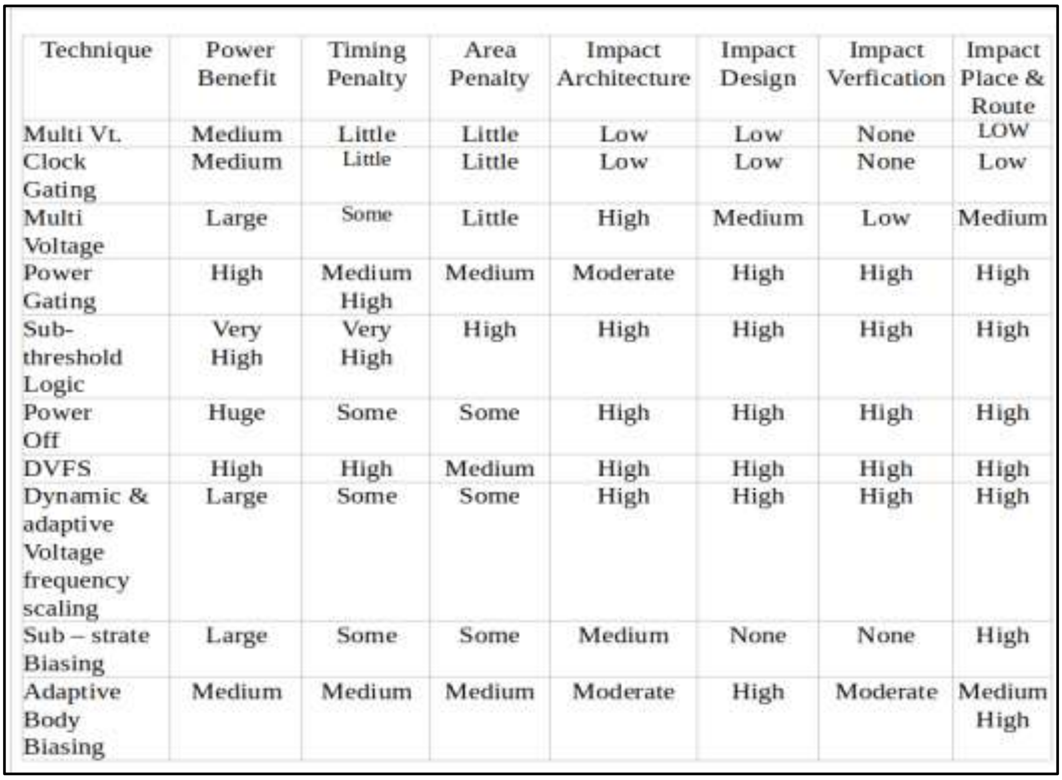


Table 1. Trade off Associated with Power Management Techniques



Technique	Power Benefit	Timing Penalty	Area Penalty	Impact Architecture	Impact Design	Impact Verfication	Impact Place & Route
Multi Vt.	Medium	Little	Little	Low	Low	None	LOW
Clock Gating	Medium	Little	Little	Low	Low	None	Low
Multi Voltage	Large	Some	Little	High	Medium	Low	Medium
Power Gating	High	Medium High	Medium	Moderate	High	High	High
Sub-threshold Logic	Very High	Very High	High	High	High	High	High
Power Off	Huge	Some	Some	High	High	High	High
DVFS	High	High	Medium	High	High	High	High
Dynamic & adaptive Voltage frequency scaling	Large	Some	Some	High	High	High	High
Sub – strate Biasing	Large	Some	Some	Medium	None	None	High
Adaptive Body Biasing	Medium	Medium	Medium	Moderate	High	Moderate	Medium High

Figure 4. Approaches to optimize power consumption of digital circuits

Sonal Bargea., 2024, “[44]”,By lowering dynamic power usage, wireless sensor nodes can become more autonomous. There are numerous low-power design strategies, and there is a lot of research being done on how the node itself may employ them automatically. In order to diminish sensor node power utilization, it develops five- state fine-grained power modes (FGPM) that modify energy usage according to the sensor node's announcement position. We use the Mica2 test bench to evaluate the proposed method. Consequently, 74.2% less power is used than with traditional methods. The suggested approach aims to lower power consumption in IoT sensor modules that run in short packet data or long sleep mode, which is how most networks function.

Tan et al., 2022, [45] In order to provide usable information, the Internet of Things lessens human intervention in data collecting and processing. To reduce power usage, it must dynamically adjust to changes in system needs

Ullah, D et.al 2024, “[46]”, IIoT and data science are integrated through data producers, analyzers, and consumers. IIoT generates vast amounts of data, from which data science uses various methods to extract crucial insights for various IoT applications and enterprises. Future study to overcome the limitations of merging IIoT and data science methodologies to improve their decision-making in real- world scenarios was suggested, based on processing, scalability, security, privacy, and decentralization. We Calculation.

1. Interaction.
2. Safety.
3. The ability to tolerate fault.

Lee et al. (2022), “[47]”,. Applications for data encryption typically require a lot of memory and processing power. SRAM is used to store the input key and enlarged keys in a low-latency, lightweight advanced encryption standard (AES) accelerator that was proposed by without a bus, the SRAM and AES accelerators may connect directly, using fewer resources and transferring data faster, which lowers energy usage.
Low-power SBox, a power gating mechanism, and a power management method are all used in Tsai et al.'s (2019) "[48]" low-power consumption AES data encryption architecture (LPADA).
See et al. (2020), “[49]”,RISC32-E, an AES-128
coprocessor built inside the RISC-V host processor, was first presented by See et al. (2020). If function-specific

hardware modules are utilized to optimize particular system features, they can lower energy usage. This article proposes a unique system that reduces energy consumption by approximately sixteen percent while increasing data processing speed.

Ko, 2022, [50],.A fault could spread throughout the connection and affect the entire system in a large-scale IoT system with heterogeneous devices and irregular connections. As a result, the IoT system requires oversight. For extensive IoT applications, a low-power, enhanced fault-tolerant CPU platform based on RISC-V is suggested. Using software-based fault tolerance can lower the overhead associated with hardware-based fault tolerance .
Fault-tolerant methods based on software that guard against soft mistakes. Target processors and hardware modification are examples of hardware features that are not taken into account by these pure software techniques. First off, little hardware changes, like adding more memory buffers, can boost the performance of software-based methods. Second, these methods are not designed for special-purpose processors like VLIW, CGRA, and GPGPU, but they can improve dependability against soft mistakes across all processors. Consequently, software- based methods that are optimized for special-purpose processors have been proposed. One such method is the use of NOPs on VLIW architectures for instruction duplication. Thus, by taking hardware issues into account, system designers can optimize the efficacy of software-based fault- tolerant solutions.

Ketan J. Raut,2021,[51], In the business world, the clock gating technique is more frequently employed. Although asynchronous processing and adiabatic logic architecture are superior options, they have numerous real- world drawbacks. Power optimization strategies at the operating system and software levels are becoming more popular these days.

Table 1 discusses the Trade off Associated with Power Management Techniques by Deepak Kumar et al 2015, [52]).

4. SUMMARY:-

While hybrid DVS offers the most efficiency at the expense of complexity, static DVS is straightforward but lacks flexibility. The particular needs of the system, workload fluctuations, and power limitations all influence the DVS selection.AI-driven next-generation power management technique called predictive DVS minimizes power waste, thermal problems, and latency by optimizing voltage scaling beforehand. It is particularly helpful for applications where power efficiency is crucial, such as cloud computing, AI hardware, HPC, and IoT. The best choices for AI and cloud computing : Cloud & AI Workload-Aware DVS and Predictive AI-based DVS.For Edge and Multi-Core AI Devices: Fine-grained control is provided by Per-Core & Per-Block Ultra-Fine-Grained DVS.For mobile devices and IoT: Easy to use and effective is Closed-Loop Adaptive DVS.The best option for 3D-IC and hybrid architectures is 3D-IC & Heterogeneous Computing DVS.Every method has compromises in terms of adaptability, efficiency, and complexity. The most sophisticated solutions, such as AI- powered predictive DVS, enable preemptive power scaling and maximum efficiency, but they also demand computational resources and AI models. Every DVS method has trade-offs between power efficiency, flexibility, and complexity.

5.RESULTS

The review paper concludes that Dynamic Voltage Scaling (DVS) is one of the most effective techniques for reducing both dynamic and leakage power in VLSI circuits. By dynamically adjusting supply voltage and operating frequency according to workload demands, DVS provides substantial energy savings without significantly compromising system performance.
The study highlights that:

- Static DVS is simple but lacks flexibility, whereas Hybrid and AI-Driven Predictive DVS provide maximum efficiency by anticipating workload requirements.
- Adaptive Voltage Scaling (AVS) further improves energy savings (up to 45%) by using closed-loop control to account for process, temperature, and workload variations.
- Combining DVS with clock gating, power gating, and multi-voltage domain design can further enhance power efficiency, reduce thermal issues, and increase memory utilization.

- Per-core and per-block fine-grained DVS is especially effective for multi-core processors and heterogeneous computing environments.
- The best-suited approaches depend on the application:
  - Cloud computing & AI hardware: Predictive AI-based DVS
  - Edge/IoT devices: Closed-loop AVS for simplicity and efficiency
  - 3D-IC / Hybrid architectures: Heterogeneous DVS for better scalability

Overall, the paper recommends AI-assisted predictive DVS as the future direction for next-generation energy-efficient VLSI systems, as it minimizes power wastage, improves thermal reliability, and ensures optimal performance across diverse workloads.

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